Final Program

ISQED

2026
27th International Symposium on

QUALITY ELECTRONIC DESIGN

AI/ML & Electronic Design, Security, IoT, Autonomous Vehicles, Quantum Computing

April 8-10, 2026
Seven Hills Conference Center
San Francisco State University
San Francisco, CA US

International Society for Quality Electronic Design

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ISQED'26 is produced and sponsored by the
International Society for Quality Electronic Design

WELCOME TO ISQED'26

It is our distinct honor to welcome you to the 27th International Symposium on Quality Electronic Design (ISQED 2026). As we move beyond last year's milestone celebration and look toward the next era of semiconductor and systems innovation, ISQED continues to serve as a premier forum dedicated to advancing the principles and practice of Quality Electronic Design in a rapidly transforming technological world.

After several years of operating in a hybrid format, this year's event places renewed emphasis on the immediacy and impact of in-person engagement at the Seven Hills Conference Center at San Francisco State University, while continuing to offer limited virtual participation for colleagues around the world. This approach fosters dynamic, face-to-face technical exchange and meaningful networking, while still accommodating those who are unable to travel due to visa constraints or cost considerations, ensuring broad and inclusive access for our global research and industry community.

For more than two decades, ISQED has championed rigorous design methodologies, system-level thinking, and cross-disciplinary collaboration in semiconductor and electronic system development. The 2026 program reflects that tradition with a carefully curated agenda featuring visionary keynotes, in-depth tutorials, a forward-looking panel discussion, and over 100 peer-reviewed technical papers selected for their innovation, relevance, and technical excellence.

Keynote Speakers

The Next Decade of Chip Design: Agentic AI and Autonomous Silicon Engineering
Dr. Houman Homayoun - Professor, University of California, Davis

Architecting the Next-generation Compute Platforms with Chiplets using Open Industry Standards
Dr. Debendra Das Sharma - Senior Fellow and Chief I/O Architect, Intel

Watermarking, Provenance, and Hardware IP Protection in Agentic AI-Based Chip Design
Dr. Farinaz Koushanfar - Professor, University of California San Diego (UCSD)

Embedded Tutorials

Advanced Packaging: Current State and Looking Forward
Dr. William Lambert, AMD

Efficient In-Memory Computing AI Chip Hardware-Software Co-Design
Prof. Deliang Fan , Arizona State University, Tempe, AZ

Panel Discussion

AI and Agentic EDA: Toward Fully Autonomous Chip Design

The 2026 program places special emphasis on transformative domains including Artificial Intelligence and Machine Learning, Agentic and Autonomous Design Systems, Advanced Packaging, IoT, Cybersecurity, and Quantum Technologies. Across three parallel tracks, participants will explore advances that bridge fundamental research and practical deployment in circuits, systems, verification, reliability, and design automation.

We are proud to continue receiving technical sponsorship from the IEEE Electron Devices Society and the IEEE Circuits and Systems Society, along with the ongoing collaboration of ACM/SigDA. As in prior years, the conference proceedings will be published in the IEEE Xplore Digital Library and indexed in Scopus, ensuring broad global visibility and long-term scholarly impact.
ISQED 2026 will take place April 8–10 (Pacific Daylight Time), with all plenary sessions, tutorials, panels, and technical presentations available both on-site and online. This dual format reflects our commitment to accessibility, diversity of participation, and meaningful global engagement.

We gratefully acknowledge the generous support of our sponsors, Innovotek and Silicon Valley Polytechnic Institute, whose partnership strengthens our ability to deliver a high-quality and impactful program. Welcome to ISQED 2026. We look forward to three days of thoughtful dialogue, technical excellence, and collaborative exploration as we continue shaping the future of quality electronic design.

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Hossein Sayadi
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The University of Tennessee, Knoxville

Special Sessions Chair
Hongyu An
Michigan Technological University

Technical Program Co- Chair
Jeff (Jun) Zhang
Arizona State University

Tutorials Chair
Na Gong
University of Alabama

ISQED Founder & Chair
Ali A. Iranmanesh
Silicon Valley Polytechnic Institute

ISQED'26 Best Papers

1A.1

Inter-Pixel Binary Edge-Detection (IPBED) Array

Md Rahatul Islam Udoy, Md Mazharul Islam, Garrett Rose, and Ahmedullah Aziz

Department of Electrical Engineering and Computer Science, University of Tennessee, Knoxville, TN 37996, USA

3B.2

Harmony: A Hardware-Mapping Co-Exploration Framework for Hybrid CIM-based Vision Transformer Accelerator

Yihang ZUO†, Zexin Fu†‡, Cong Wang†, Yuchao Wu†, Jiayi Huang†, Yuzhe Ma†

†Thrust of Microelectronics, Hong Kong University of Science and Technology (Guangzhou)

‡Guangdong-Macao Joint Laboratory for Modular Chip Design and Testing, Hong Kong University of Science and Technology (Guangzhou)

5C.2

A Low-Power Analog Spiking Neural Network with On-Chip Learning

Kiruthikan Sithamparanathan, Jeff DixKiruthikan Dix

Department of Electrical Engineering and Computer Science

University of Arkansas, Fayetteville, Arkansas, USA

Authors of best papers are acknowledged during the morning plenary session on Wednesday April 8.
ISQED'26 best papers are sponsored by **Silicon Valley Polytechnic Institute**.

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Arizona State University

Tutorials Chair
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Publication Chair
Paul Wesling
Hewlett Packard (retired)

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Cognitive Computing Hardware (CCH)

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Committee Members:
Hongyu An - Michigan Technological University
Kang Jun Bai - Air Force Research Laboratory
Haowen Fang - NCTIEDA
Darshan Gandhi - Sambanova Systems Inc
Shaoyi Huang - Stevens Institute of Technology
Doo Seok Jeong - Hanyang University
Hao Jiang - San Francisco State University
Mehdi Kamal - University of Southern California
Sunny Raj - Oakland University
Gopal Raut - Khalifa University
Ao Ren - Chongqing University
Banafsheh Saber Latibari - University of Arizona
Ishan Thakkar - University of Kentucky
Cindy Yang Yi - Virginia Tech
Miao Yin - University of Texas at Arlington

Design Test and Verification (DTV)

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Jay Dholakia - AMD
Michael Hsiao - Virginia Tech
Chrysovalantis Kavousianos - Department of Computer Science and Engineering, University of Ioannina
Dimitris Nikolos - University of Patras
Sushant Sadangi - Intel Corporation
Vikas Singh - Omni Design Technologies
Yiorgos Tsiatouhas - University of Ioannina
Miroslav Velev - Aries Design Automation
Arnaud Virazel - LIRMM

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Abishai Daniel - Micron
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Xinfei Guo - Shanghai Jiao Tong University
Sandeep Hari - Samsung
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Zhixing Li - Synopsys
Zizhen Liu - Institute of Computing Technology,Chinese Academy of Sciences
Ofelya Manukyan - NA
Rajeev Murgai - Cadence India
Murthy Palla - Synopsys Inc.
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Jia Wang - Illinois Institute of Technology
Hua Xiang - IBM Research
Richard Yarnell - University of Central Florida
Huan Yu - Apple
Rui Zhang - Cadence Design Systems
Lining Zhang - Peking University

System-level Design and Methodologies (SDM)

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Iraklis Anagnostopoulos - Southern Illinois University Carbondale
Eshan Bhatia - Nvidia
Kunvar Chokshi - Tesla Inc.
Andrea Guerrieri - EPFL and HES-SO
Fabiano Hessel - PUCRS
Hana Kubatova - Czech Technical University in Prague
Huizhang Luo - Hunan Univeristy
Mikhail Moiseev - Intel
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Maruthi Mukkannaiah - iota Biosciences
Vojin Oklobdzija - University of California Davis
Praveen Prabha - Astera Labs
Suyash Ranjan - Qualcomm
Sudipta Sarkar - Cadence Design Systems
Thilo Sauter - Danube University Krems
Ali Shahi - LogicWise AI
Yanchao Wang - Broadcom
zhichao Zhang - Intel
Zhen Zhou - Intel Corp

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Hongyu An, Michigan Technological University (Chair)

TECHNICAL PROGRAM COMMITTEES
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Tasnuva Farheen - Louisiana State University
Farah Ferdaus - Lamar University
Dominik Germek - Corporate Research Robert Bosch GmbH
Najmeh Nazari - UC Davis
Md Tauhidur Rahman - Florida International University
Biswajit Ray - Colorado State University
Francesco Regazzoni - University of Amsterdam and Università della Svizzera italiana
fareena saqib - University of North Carolina at Charlotte
Zhijie Shi - University of Connecticut
Nicolas Sklavos - University of Patras
Benjamin Tan - University of Calgary
Jiliang Zhang - Hunan University

Emerging Device and Process Technologies and Applications (EDPT)

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Vita Pi-Ho Hu - National Taiwan University
Huamin Li - University at Buffalo
Kexin Li - Arizona State University
Chun-Yu Lin - National Yang Ming Chiao Tung University
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Zhaohao Wang - Beihang University
Heng Wu - Peking University
Mustafa Berke Yelten - Istanbul Technical University

GENERAL INFORMATION
ISQED'26

April 8-10, 2026
Seven Hills Conference Center
San Francisco State University

AWARDS & RECOGNITIONS

Wednesday April 8, 8:40 AM - 9:00 AM
Track A - Nob Hill Room

Best Paper Awards

Recipients of the ISQED'26 Best Paper Awards will be recognized in this segment of the program. The best papers are shown in Page 2 of this document.

Keynotes

Keynote 1P.1

Wednesday, April 8, 9:00 AM - 9:35 AM

The Next Decade of Chip Design: Agentic AI and Autonomous Silicon Engineering

Dr. Houman Homayoun - Professor, University of California, Davis

Keynote 1P.2

TWednesday, April 8, 11:40 AM - 12:15 PM

Watermarking, Provenance, and Hardware IP Protection in Agentic AI-Based Chip Design

Dr. Farinaz Koushanfar, Professor, University of California San Diego (UCSD)

Keynote 2P.1

Thursday, April 9, 9:00 AM - 9:35 AM

Architecting the Next-generation Compute Platforms with Chiplets using Open Industry Standards

Dr. Debendra Das Sharma - Senior Fellow and Chief I/O Architect, Intel

Panel Discussion

Wednesday, April 8, 3:15 PM - 4:45 PM
Track A - Nob Hill Room

AI and Agentic EDA: Toward Fully Autonomous Chip Design

Artificial intelligence is rapidly transforming electronic design automation—from rule-based optimization and predictive analytics to agentic systems capable of reasoning, planning, and acting across complex design spaces. As large language models, reinforcement learning, and multi-agent frameworks mature, a fundamental question emerges: Can chip design become fully autonomous? This panel brings together leaders from industry and academia to examine the promise and limits of agentic EDA. We will explore how autonomous agents may reshape front-end design, physical implementation, verification, and manufacturing handoff—and whether such systems can truly replace, or only augment, human designers. Panelists will debate technical readiness, trust, verification, accountability, intellectual property concerns, and the changing role of designers in an era of machine-driven decision-making. By contrasting near-term deployable capabilities with long-term visions, this panel aims to clarify what "autonomous chip design" realistically means, what obstacles remain, and how the EDA ecosystem must evolve to responsibly harness agentic intelligence.

Modedrator & Chair:
Dr. Ahmedullah Aziz - University of Tennessee Knoxville

Panelists:
Dr. Chia-Tung (Mark) Ho
Senior Research Scientist at Nvidia
Dr. Souvik Kundu
Senior Staff Research Scientist at Intel Labs
Dr. Houman Homayoun
Professor - University of California, Davis

Embedded Tutorials

Chair & Moderators:
Na Gong - University of Alabama (Chair)

Track A - Nob Hill Room

Tutorial 1
Wednesday, April 8, 12:25 PM -1:25 PM

Advanced Packaging: Current State and Looking Forward

Dr. William Lambert
AMD

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Tutorial 2
Thursday April 9, 1:05 PM -2:05 PM

Efficient In-Memory Computing AI Chip Hardware-Software Co-Design

Prof. Deliang Fan
Arizona State University, Tempe, AZ

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TECHNICAL SESSIONS

There are a total of 24 paper sessions held on Wednesday to Friday. Technical sessions are held in the format of three parallel tracks **A, B, C** located respectively in Nob Hill Room, Russian Hill Room, and Mt. Davidson room.

ON-SITE REGISTRATION

Tentative time schedule of on-site registration is as follows:

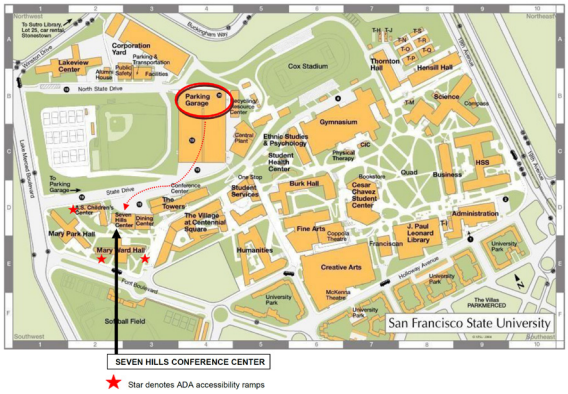
Wednesday, April 8, 8:00 AM - 2:00 PM
Thursday , April 9, 8:00 AM -11:00 AM

Registration desk location will be at the conference center lobby.

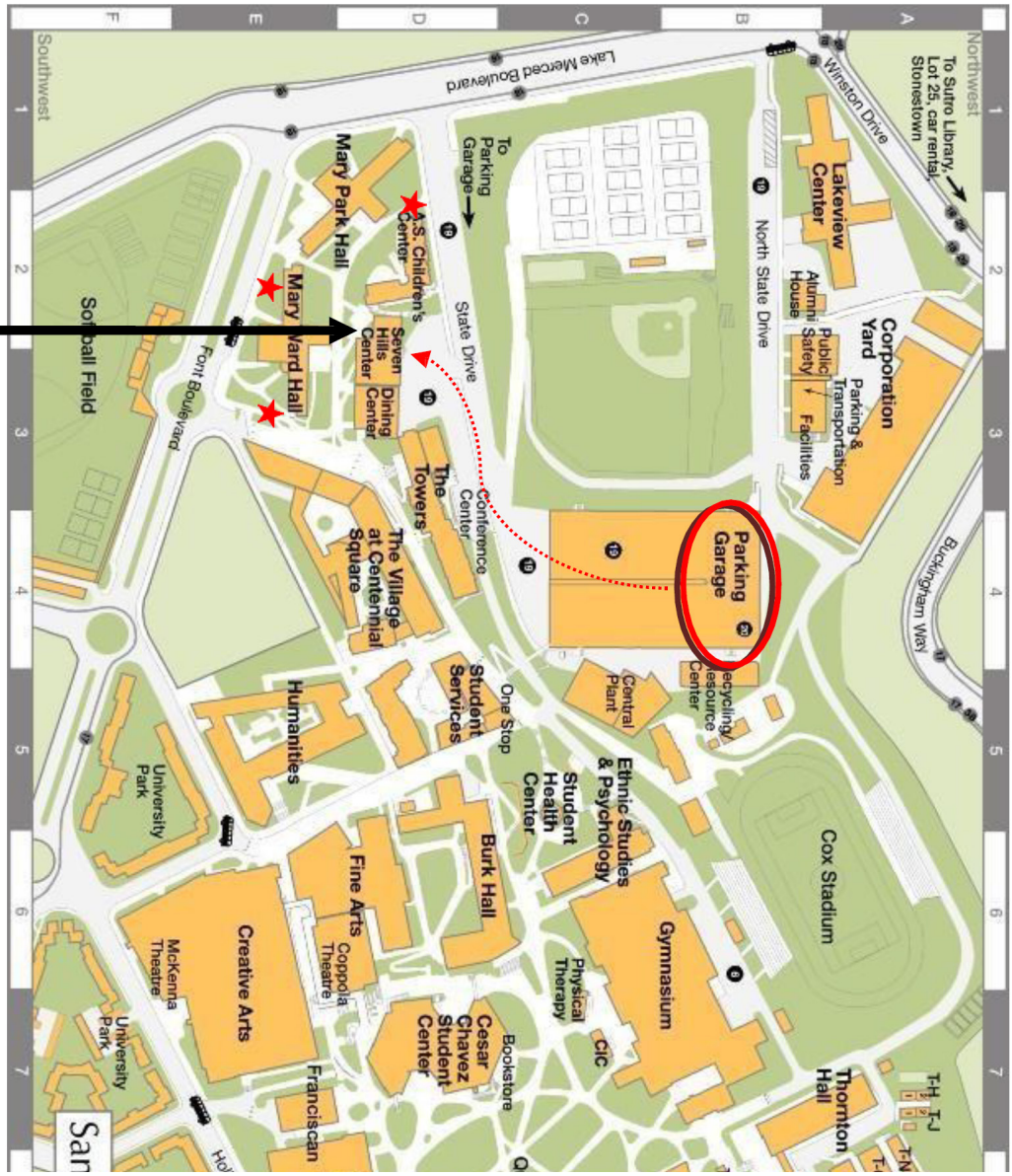
Seven Hills Conference Center

ISQED'26 conference will be held in Seven Hills Conference Center, located in San Francisco State University, 800 Font Blvd, San Francisco, CA 94132.

If you are using navigator the best address to use is: 796 state drive, San Francisco, CA 94132. (Note: make sure to use Google Maps app) At the end of State Drive is the Public Parking Lot ("Lot 20"). Parking is $6.25 for less than 2 hours, and $10 for 2+ hours. Pay stations on each floor accept $1, $5 and $10 bills as well as credit/debit cards. Be advised, pay stations do not provide change. Please have exact amount. From the garage, Seven Hills' entrance can be accessed from State Drive by walking Southwest towards the A.S. Children's Center and taking the staircase beside it up one flight. Wheelchair access: go past the A.S. Children's Center and take a left onto the path. Follow to the entrance to the Seven Hills Conference Center.



UNIVERSITY MAP & CONFERENCE CENTER LOCATION+



WEDNESDAY APRIL 8

	Plenary Session 1: (Track A- Nob Hill Room)		
8:40am–9:00am	**Introduction, Committee Recognitions, Best Paper Awards**		
9:00am-9:35am	**Keynote:** The Next Decade of Chip Design: Agentic AI and Autonomous Silicon Engineering **Dr. Houman Homayoun - Professor, *University of California, Davis***		
9:35am–10:10am			
10:10am–10:20am	**Break**		
10:20am–11:40am	**Session 1A (Nob Hill Room)** **Emerging Transistors and Circuits**	**Session 1B (Russian Hill Room)** **Foundations of Cryptographic Hardware Security**	**Session 1C (Mt. Davidson Room)** **From Specifications to Silicon: Advanced Verification Across the Hardware Stack**
11:40am-12:25pm	**Lunch Break** **Keynote:** Watermarking, Provenance, and Hardware IP Protection in Agentic AI-Based Chip Design **Dr. Farinaz Koushanfar - Professor, *University of California San Diego (UCSD)***		
12:25pm-13:25am	**Embedded Tutorial 1 (Track A)** Advanced Packaging: Current State and Looking Forward *Presenter:* Dr. William Lambert, AMD		
13:25pm-13:30pm	**Break**		
13:30pm-15:10pm	**Session 2A (Nob Hill Room)** **AI and Machine Learning in Hardware Design**	**Session 2B (Russian Hill Room)** **Detection, Validation, and Reverse Engineering of Malicious Hardware**	**Session 2C (Mt. Davidson Room)** **AI & Machine Learning Acceleration – Architectures and Co-Design**
15:10pm-15:15pm	**Break**		
15:15pm-16:45pm	**Panel Discussion - (Track A - Nob Hill Room)** AI and Agentic EDA: Toward Fully Autonomous Chip Design *Chair:* Dr. Ahmedullah Aziz *Panelists:* Dr. Chia-Tung (Mark) Ho, Dr. Souvik Kundu, Dr. Houman Homayoun		

THURSDAY APRIL 9

	Plenary Session 2: (Track A - Nob Hill Room)		
8:45am–9:00am	**Welcome**		
9:00am–9:35am	**Keynote:** **Architecting the Next-generation Compute Platforms with Chiplets using Open Industry Standards** **Dr. Debendra Das Sharma - Senior Fellow and Chief I/O Architect, *Intel***		
9:35am–9:40am	**Break**		
9:40am-10:35am	**Session PW1 (Nob Hill Room, Track A)** **Short Presentation & WIP Session 1**	**Session PW2 (Russian Hill Room, Track B)** **Short Presentation & WIP Session 2**	**Session PW3 (Mt. Davidson Room, Track C)** **Short Presentation & WIP Session 3**
10:35am-10:45am	**Break**		
10:45am–12:25pm	**Session 3A (Nob Hill Room)** **Advanced Circuit Modeling and Analysis**	**Session 3B (Russian Hill Room)** **NN Acceleration & Dataflow Optimization**	**Session 3C (Mt. Davidson Room)** **Security for AI and AI for Security**
12:25pm-13:05	**Lunch Break** **Agentic AI Design Verification Challenge 2026**		
13:05pm-14:05pm	**Embedded Tutorial 2 (Track A - Nob Hill Room)** **Efficient In-Memory Computing AI Chip Hardware-Software Co-Designs** *Presenter:* Prof. Deliang Fan , Arizona State University		
14:05pm-14:10pm	**Break**		
14:10pm-15:50pm	**Session 4A (Nob Hill Room)** **Innovative Design Methodologies and Frameworks**	**Session 4B (Russian Hill Room)** **Fault, Memory, and Physical Attacks on Hardware Systems**	**Session 4C (Mt. Davidson Room)** **Neuromorphic Computing**

FRIDAY APRIL 10

8:40am-10:20am	**Session 5A** (Nob Hill Room) Quantum and memory technology and circuits	**Session 5B** (Russian Hill Room) Memory Systems, Approximate Computing, and System-Level Optimization	**Session 5C** (Mt. Davidson Room) Neuromorphic and Approximate Computing Hardware for Next-Generation AI
10:20am-10:30am	Break		
10:30am–12:10pm	**Session 6A** (Nob Hill Room) Timing and Placement Optimization Techniques	**Session 6B** (Russian Hill Room) Security and Robustness of Machine Learning Hardware	**Session 6C** (Mt. Davidson Room) Emerging AI workloads on NPUs
12:10pm-12:55	Lunch Break		
12:55pm-14:35pm	**Session 7A** (Nob Hill Room) Hyperdimensional, Neuromorphic, and Robust Cognitive Computing Hardware	**Session 7B** (Russian Hill Room) System-Level and Supply-Chain Security for Trusted Computing	**Session 7C** (Mt. Davidson Room) EdgeAI and Applications

ISQED Keynote 1P.1

Wednesday April 8

9:00 AM - 9:35 AM

Room: Nob Hill

The Next Decade of Chip Design: Agentic AI and Autonomous Silicon Engineering

Dr. Houman Homayoun

Professor, University of California, Davis

Recent advances in large language models have accelerated the adoption of AI in chip design, enabling new forms of assistance for RTL generation, verification, and debugging. However, most existing AI-driven EDA approaches remain limited to prompt-based interaction and isolated task execution, lacking the ability to reason over long design horizons, coordinate across tools, or adapt to complex, evolving design states. As semiconductor systems grow in scale and heterogeneity—and as technology nodes continue to shrink—these limitations increasingly constrain the impact of AI on reducing design time, verification effort, and overall development risk. This talk focuses on the emerging paradigm of agentic AI for chip design, where collections of specialized, interacting agents operate over specifications, RTL, verification environments, and EDA tools to plan, execute, verify, and refine design decisions. We discuss how orchestration of LLMs and domain-specific small language models (SLMs), combined with tool invocation, function calling, retrieval-augmented reasoning, and persistent design memory, is enabling new capabilities in design verification (UVM, formal property generation, regression triage), specification-driven RTL generation, and security-aware design flows. The presentation highlights how agentic frameworks can embed trust, correctness, and security considerations directly into the generation and verification process, enabling early detection of vulnerabilities and systematic reasoning about design intent—pointing toward a future of more autonomous, scalable, and trustworthy chip design workflows.

About Houman Homayoun

Houman Homayoun is currently a Professor in the Department of Electrical and Computer Engineering at the University of California, Davis. He is also the director of the National Science Foundation Center for Hardware and Embedded Systems Security and Trust (CHEST). Before that, he was an Associate Professor in the Department of Electrical and Computer Engineering at George Mason University (GMU). From 2010 to 2012, he spent two years at the University of California, San Diego, as NSF Computing Innovation (CI) Fellow awarded by the CRA-CCC. Houman graduated in 2010 from the University of California, Irvine, with a Ph.D. in Computer Science. He was a recipient of the four-year University of California, Irvine Computer Science Department chair fellowship. Houman received an MS degree in computer engineering in 2005 from the University of Victoria and a BS degree in electrical engineering in 2003 from the Sharif University of Technology. Houman conducts research in hardware security and trust, applied machine learning and AI, data-intensive computing, and heterogeneous computing, where he has published more than 200 technical papers in prestigious conferences and journals on the subject and directed over $10M in research funding from NSF, DARPA, AFRL, NIST, US Congress, and various industrial sponsors. His work received several best paper awards and nominations in various conferences, including GLSVLSI 2016, ICCAD 2019, ICDM 2019, DCAS 2020, ISVLSI 2020, ICCAD 2020, DATE 2022. His CHEST center received congressional support for research in HW security which was included in 2021 National Defense Authorization Act. Houman served as a Member of the Advisory Committee, Cybersecurity Research and Technology Commercialization working group in the Commonwealth of Virginia. He also served as core group member of the hardware security body of knowledge development team supported by the Department of Defense. He was a recipient of the 2010 National Science Foundation computing innovation fellow award by CCC/CRA. Since 2017 he has been serving as an Associate Editor of IEEE Transactions on VLSI. He chaired and co-chaired major conferences in ACM, including Great Lake Symposium on VLSI.

ISQED Keynote 1P.2

Wednesday April 8

11:40 AM - 12:15 PM

Room: Nob Hill

Watermarking, Provenance, and Hardware IP Protection in Agentic AI-Based Chip Design

Dr. Farinaz Koushanfar

Professor, University of California San Diego (UCSD)

Generative LLMs and agentic AI systems are increasingly vital in SoC and hardware design flows, where autonomous agents generate RTL and optimize physical layouts. Ensuring provenance—the ability to trace the origin and modification history of AI-generated design artifacts—is critical for IP protection. This talk focuses on watermarking techniques for models and their artifacts, with special emphasis on protecting hardware intellectual property. We explore how agentic workflows embed verifiable provenance trails, enabling designers to detect unauthorized use and prevent IP theft in collaborative EDA toolchains. We show how such systems can be further leveraged for hardware-based attestation. We demonstrate practicality and low overhead of these methods on real IC design flows and benchmarks. Finally, we discuss current limitations and future research for responsible deployment of generative AI in semiconductor design, safeguarding the most valuable IP assets.

About Farinaz Koushanfar

Farinaz Koushanfar is the Nemati-Nasser Endowed Professor of Electrical and Computer Engineering (ECE) at the University of California San Diego (UCSD), where she is the founding co-director of the UCSD Center for Machine-Intelligence, Computing & Security (MICS). She is also a research scientist at Chainlink Labs. She received her PhD in Electrical Engineering and Computer Science, as well as an MA in Machine Learning and Statistics from UC Berkeley. Her research addresses several aspects of automated and secure design automation, with a focus on AI-based optimization, agentic systems, robust machine learning under resource constraints, hardware and system security, intellectual property (IP) protection, as well as privacy-preserving computing. Dr. Koushanfar has received several awards and honors for her research, including a number of best paper awards, MIT TR-35 (World's top innovators under 35) and the PECASE Presidential Award from President Obama. She is a fellow of AAAS, ACM, IEEE, the National Academy of Inventors (NAI), and the Kavli Frontiers of the National Academy of Sciences (NAS).

ISQED Keynote 2P.1

Thursday April 9

9:00 AM - 9:35 AM

Room: Nob Hill

Architecting the Next-generation Compute Platforms with Chiplets using Open Industry Standards

Dr. Debendra Das Sharma

Senior Fellow and Chief I/O Architect, Intel

The next era of computing demands annual exponential performance growth within strict power and cost limits, driven by AI, machine learning, autonomous driving, and IoT applications. Achieving this requires a new paradigm of on-package integration of chiplets for heterogeneous compute, high-bandwidth memory, and advanced communication in an energy-efficient architecture. The chiplet revolution is accelerating this transformation. The chiplet market is projected to exceed $400 billion by 2035 at a 15.7% CAGR (IDTechEx, 2024), and IBS (2023) estimates that over half of all new silicon design starts will use chiplets. At the heart of this movement, the Universal Chiplet Interconnect Express (UCIe) has rapidly emerged as the open standard for seamless, low-power, high-bandwidth on-package communication. A Synopsys (2025) survey shows UCIe in 97% of chiplet designs; over 50% in AI, HPC, and servers, 20% in automotive, and the rest across consumer, storage, and edge devices. With a power efficiency of 0.25 pJ/bit for planar, delivering 1.5 TB/s/mm2, and 0.01 pJ/bit for vertical interconnects, delivering over 100 TB/s/ mm2, UCIe provides orders of magnitude improvement in both power efficiency and bandwidth density over external interconnects like PCI-Express and Ethernet. This keynote explores how UCIe is shaping the next generation of secure, manageable, and scalable systems, driving innovation from cloud to edge, and laying the foundation for a sustainable, intelligent, and interconnected future.

About Debendra Das Sharma

Dr. Debendra Das Sharma is an Intel Senior Fellow and Chief I/O Architect, Platform Engineering Group, at Intel Corporation. He is a member of NAE, Fellow of IEEE, and Fellow of International Academy of AI Sciences (AAIS). He is a leading expert on I/O subsystem and interface architecture. He delivers Intel-wide critical interconnect technologies in Peripheral Component Interconnect Express (PCIe), Compute Express Link (CXL), Universal Chiplet Interconnect Express (UCIe), and Intel's Coherency interconnect, as well as their implementation. Dr. Das Sharma is a member of the Board of Directors and treasurer for the PCI Special Interest Group (PCI-SIG). He has been a lead contributor to PCIe specifications since its inception. He is the co-inventor of CXL, a founding member of the CXL consortium, and chairs the CXL consortium. He co-led the CXL Board Technical Task Force (2019-2024), and is a leading contributor to CXL specifications. He co-invented the chiplet interconnect standard UCIe and is the chair of the UCIe consortium. Dr. Das Sharma has a bachelor's in technology (with honors) degree in Computer Science and Engineering from the Indian Institute of Technology, Kharagpur and a Ph.D. in Computer Engineering from the University of Massachusetts, Amherst. He holds 230+ US patents and 500+ patents world-wide. He is a frequent keynote/ plenary speaker, distinguished lecturer, invited speaker, invited columnist, and panelist at Nature Electronics, IEEE International Test Conference, IEEE Hot Interconnects, IEEE Cool Chips, IEEE 3DIC, SNIA SDC, PCI-SIG Developers Conference, CXL consortium, Open Server Summit, Open Fabrics Alliance, Flash Memory Summit, Intel Innovation, and Universities (CMU, Texas A&M, Georgia Tech, UIUC, UC Irvine). He has been awarded the Distinguished Alumnus Award from Indian Institute of Technology, Kharagpur in 2019, the IEEE Region 6 Outstanding Engineer Award in 2021, the first PCI-SIG Lifetime Contribution Award in 2022, the IEEE Circuits and Systems Industrial Pioneer Award in 2022, and the IEEE Computer Society Edward J. McCluskey Technical Achievement Award in 2024.

Panel Discussion

Wednesday April 8

3:25 PM–4:55 PM

Room: Nob Hill

AI and Agentic EDA: Toward Fully Autonomous Chip Design

Panelists:

Dr. Chia-Tung (Mark) Ho - Senior Research Scientist at Nvidia

Dr. Souvik Kundu - Senior Staff Research Scientist at Intel Labs

Dr. Houman Homayoun - Professor - University of California, Davis

Modedrator/Chair:

Dr. Ahmedullah Aziz - University of Tennessee Knoxville

Summary:
Artificial intelligence is rapidly transforming electronic design automation—from rule-based optimization and predictive analytics to agentic systems capable of reasoning, planning, and acting across complex design spaces. As large language models, reinforcement learning, and multi-agent frameworks mature, a fundamental question emerges: Can chip design become fully autonomous? This panel brings together leaders from industry and academia to examine the promise and limits of agentic EDA. We will explore how autonomous agents may reshape front-end design, physical implementation, verification, and manufacturing handoff—and whether such systems can truly replace, or only augment, human designers. Panelists will debate technical readiness, trust, verification, accountability, intellectual property concerns, and the changing role of designers in an era of machine-driven decision-making. By contrasting near-term deployable capabilities with long-term visions, this panel aims to clarify what "autonomous chip design" realistically means, what obstacles remain, and how the EDA ecosystem must evolve to responsibly harness agentic intelligence.

Wednesday April 8

12:25 AM - 1:25 PM

Nob Hill Room

Advanced Packaging: Current State and Looking Forward

Dr. William Lambert

AMD

Summary:

Advanced packaging is now an essential component of high-performance SOC design, spanning applications from low-cost consumer CPUs to leading-edge AI processors. For AI applications in particular, advanced packaging is indispensable – it is the only way to enable the integration of large compute area, high memory capacity, and massive memory bandwidth required for competitive products. This tutorial will provide an overview of advanced packaging strategies currently in use, including hybrid bond stacking, silicon interposer, and fan-out bridge technologies, with a focus on their implementation in AMD products. Next, future directions for scaling these technologies will be reviewed with an emphasis on how new concepts in SOC architecture and circuit design may drive "Design Technology Co-Optimization" (DTCO) in years to come. Finally, the tutorial will review how adjacent areas are developing to support the disaggregated designs enabled by advanced packaging, including package and silicon design and verification tools, electrical and mechanical simulation tools, sort, and test.

About William Lambert

William Lambert is a Fellow of AMD, Inc. where he leads a team creating the packaging solutions for next-generation AI products. He previously worked on packaging solutions for datacenter and client GPUs and CPUs. Prior to joining AMD, he was a Senior Principal Engineer in the Assembly & Test Technology Development group at Intel Corporation, where he held leadership roles in packaging architecture definition, power delivery and integrated voltage regulation technology development, and RF packaging development. He received his Ph.D. in electrical engineering from Arizona State University with a focus on low-voltage DC-DC power electronics for computer systems, and his M.S. and B.S. degrees from Rochester Institute of Technology.

Thursday April 9

1:05 PM - 2:05 PM

Nob Hill Room

Efficient In-Memory Computing AI Chip Hardware-Software Co-Design

Prof. Deliang Fan

Arizona State University, Tempe, AZ

Summary:

In-memory computing is becoming a promising solution to overcome the well-known 'memory-wall' challenge, through directly processing the data within memory where data is stored. Therefore, it will reduce massive power hungry data traffic between computing and memory units, leading to significant improvement of entire system performance and energy efficiency. Many different memory technologies have been explored for the design of compute-in-memory (CIM) or in-memory computing (IMC), such as emerging post-CMOS Magnetic Random Access Memory (MRAM), Resistive RAM (ReRAM), or silicon based Static Random Access Memory (SRAM) and Dynamic RAM (DRAM), etc. In this talk, Prof. Deliang Fan, from Arizona State University (ASU), will present state-of-the-art research in energy efficient and intelligent cross-layer in-memory computing AI chip design spanning from new memory technologies, compute-in-memory circuit & chip design demos, and hardware-aware AI model optimization.

About Deliang Fan

Dr. Deliang Fan is currently an Associate Professor in the School of Electrical, Computer and Energy Engineering, Arizona State University, Tempe, AZ, USA. He received his M.S. and Ph.D. degrees in Electrical and Computer Engineering from Purdue University, West Lafayette, IN, USA, in 2012 and 2015, respectively. Dr. Fan's primary research interests include AI Hardware, Digital Chip Design, Efficient AI algorithm, In-Memory Computing Circuits and Architecture, Adversarial and Trustworthy AI System. Dr. Fan is the co-founder of an AI chip startup. Dr. Fan has authored around 190 peer-reviewed international journal/conference research papers. He is the receipt of National Science Foundation Career Award, best paper award of 2019 ACM Great Lakes Symposium on VLSI, 2018 IEEE Computer Society Annual Symposium on VLSI (ISVLSI), and 2017 IEEE ISVLSI, best IP paper award of 2022 Design Automation and Test in Europe (DATE). His research works were also nominated as best paper candidate 2021 Design Automation Conference (DAC), 2019 Asia and South Pacific Design Automation Conference (ASPDAC) and 2019 International Symposium on Quality Electronic Design (ISQED). He is also the TPC Chair/Co-Chair of ISQED 2023-2026, chair of iMACAW@DAC 2022-2025, technical area chair of DAC 2021/2025, GLSVLSI 2019-2022, ISQED 2019-2022. He served as technical reviewers for 30+ international journals/conferences, such as Nature Electronics, IEEE TNNLS, TVLSI, TCAD, TNANO, TC, TCAS, etc. He also served as the Technical Program Committee member of DAC, ICCAD, HPCA, MICRO, AAAI, WACV, GLSVLSI, ISVLSI, ASP-DAC, etc. Dr. Fan served as the guest editor of IEEE Transactions on Very Large Scale Integration Systems (TVLSI), IEEE Journal on Emerging and Selected Topics in Circuits and Systems, IEEE Transactions on Emerging Topics in Computing (TETC), Frontiers in Physics, etc. Dr. Fan is a senior member of IEEE and ACM. Please refer to his research website for more details: https://faculty.engineering.asu.edu/dfan/

SESSION 1A

Wednesday April 8

Emerging transistors and circuits

Chair: **Rasit Topaloglu**, Adeia

10:15AM
1A.1
52 **Inter-Pixel Binary Edge-Detection (IPBED) Array**
Md Rahatul Islam Udoy[1], Md Mazharul Islam[2], Garrett Rose[1], Ahmedullah Aziz[1]
[1]University of Tennessee, Knoxville, [2]The University of Tennessee

10:35AM
1A.2
137 **Fault Tolerant Design of IGZO-based Binary Search ADCs**
Paula Lozano Duarte[1], Sule Ozev[2], Mehdi Tahoori[1]
[1]Karlsruhe Institute of Technology, [2]ASU

10:55AM
1A.3
105 **Thermal-Aware Compact Modeling and Design-Space Exploration of δ-Doped β-Ga2O3 MOSFETs for RF Power Electronics**
Habibullah Khan, Nabasindhu Das, Nidhin Kurian Kalarickal, Kexin Li
Arizona State University

11:15AM
1A.4
139 **Temperature-Dependent Current–Voltage Model for Emerging GAA NS FETs Using a Physics-Inspired Neural Network**
Yiming Li, Yun Tai, Min-Hui Chuang
National Yang Ming Chiao Tung University

11:35AM

1A.5

144 **Pioneering the Use of Response Surface Modeling for Complementary Field-Effect Transistors Design and Optimization**

Yu-Wen Xu and Yiming Li
National Yang Ming Chiao Tung University

SESSION 1B

Wednesday April 8

Foundations of Cryptographic Hardware Security

Chair: **Sergiu Mosanu**, University of Virginia

10:15AM

1B.1

OK-BMM: A Power-Performance-Efficient Overlap-Free Karatsuba Based Barrett Modular Multiplier for Secure Embedded Systems

77 *Bhavana S[1], Keerthana B[2], Madhav Rao[3]*

[1]International Institute of Information Technology, Bangalore, [2]International Institute of Information Technology Bangalore, [3]International Institute of Information Technology-Bangalore

10:35AM

1B.2

R-BMM: A Reconfigurable Barrett Modular Multiplier Architecture for High-Performance Cryptographic Systems

147 *Keerthana B[1], Bhavana S[2], Madhav Rao[3]*

[1]International Institute of Information Technology Bangalore, [2]International Institute of Information Technology, Bangalore, [3]International Institute of Information Technology-Bangalore

10:55AM

1B.3

A Low-overhead Dilithium-NTT Architecture using Accelerated K-RED Modular Reduction Unit

92 *Harsh Gupta[1], Aryan Goyal[1], Paranjay Dhadwal[1], Jugal Gandhi[2], Diksha Shekhawat[3], M. Santosh[4], Jai Gopal Pandey[4]*

[1]Birla Institute of Technology and Science (BITS) Pilani Goa Campus, [2]AcSIR at CSIR-CEERI, [3]AcSIR, CSIR-CEERI, [4]CSIR -Central Electronics Engineering Research Institute (CEERI), Pilani, Rajasthan, India

11:15AM

1B.4

STREAMLOCK: Stream Cipher-Enabled Cryptographic Logic Locking

196 *Nahush Tambe[1], DHRUVAKUMAR AKLEKAR[2], Naseeruddin Lodge[2], Vineet Chadalavada[3], fareena saqib[2]*

[1]University f North Carolina at Charlotte, [2]UNIVERSITY OF NORTH CAROLINA AT CHARLOTTE, [3]UNC Charlotte

11:35AM

1B.5

128 **Hardware-Efficient Compound IC Protection with Lightweight Cryptography**

Levent Aksoy[1], Muhammad Munir[1], Sedat Akleylek[2]

[1]Tallinn University of Technology, [2]University of Tartu

SESSION 1C

Wednesday April 8

From Specifications to Silicon: Advanced Verification Across the Hardware Stack

Chair: **Chidhambaranathan Rajamanikkam**, Synopsys

10:15AM
1C.1
14 **Specification-Driven INL Generation for Behavioral ADC Models with Controlled Error Injection**
Thorben Schey[1], Khaled Karoonlatifi[2], Michael Weyrich[1], Andrey Morozov[1]
[1]University of Stuttgart, [2]Advantest Europe GmbH

10:35AM
1C.2
Verifying Hardware Resource Isolation Using Mandatory Access Control
11 *Christopher Nokes[1], Kostas Amberiadis[2], D. Richard Kuhn[3], Edwards Reed[4], Michael Zuzak[1]*
[1]Rochester Institute of Technology, [2]National Institute of Standards and Technology, [3]Virginia Tech, [4]AESEC Global Services, Inc.

10:55AM
1C.3
177 **Scalable Hardware–Software Co-Verification through Linux Driver Reuse: Methodology Validated on USB4 and xHCI Host Controllers.**
Suchir Gupta, Amit Sharma, Suneetha Suryadevara, Vishnuvardhan mandala
Synopsys

11:15AM
1C.4
21 **Cutwidth Decomposition on Circuit-AIGs: Taming Verification Complexity of Arithmetic Circuits**
Luca Müller[1], Mohamed Nadeem[2], Rolf Drechsler[1]
[1]University of Bremen/DFKI, [2]University of Bremen

SESSION 2A

Wednesday April 8

AI and Machine Learning in Hardware Design

Chair: **Sergiu Mosanu**, University of Virginia

1:40PM
2A.1
4 **BPINN-EM-Post: Bayesian Physics-Informed Neural Network based Stochastic Electromigration Damage Analysis in the Post-void Phase**
Subed Lamichhane[1], Haotian Lu[1], Sheldon Tan[2]
[1]University of California, Riverside, [2]University of California at Riverside

2:00PM
2A.2
AutoBeaVer: Automating Behavioral Modeling and Verification in Library
18 **Characterization with LLM Agents**
Tianze Wu[1], Jian Xin[2], Yuan Wang[2], Xuliang Yu[1], Xunzhao Yin[1], Qianqian Yang[1], Zuochang Ye[2], Liang Zhao[1]
[1]Zhejiang University, [2]Tsinghua University

2:20PM

2A.3

22 **HeXinTimer: An AI-Enhanced STA Framework Supporting CCS and SI with Signoff Accuracy**

Chao Yan[1], Zishu Wu[1], Jingjia Xu[1], Boyuan Liu[2], Xi Chen[1], Zefeng Wang[3]

[1]Hexin, [2]Zhejiang University, [3]Huzhou University

2:40PM

2A.4

134 **Integrating Automatic Prompt Engineering and Vision-Language Model for Pad Defect Classification**

Yi-Ting Shen[1], Yan-Hsiu Liu[2], Yi-Ting Li[1], Wuqian Tang[1], Yung-Chih Chen[3], Hao-Chiang Shao[4], Chia-Wen Lin[1], Chun-Yao Wang[1]

[1]National Tsing Hua University, [2]United Microelectronics Corporation, [3]National Taiwan University of Science and Technology, [4]National Chung Hsing University

3:00PM

2A.5

194 **Accelerating Post-Quantum Cryptography via LLM-Driven Hardware-Software Co-Design**

Yuchao Liao, Tosiron Adegbija, Roman Lysecky

University of Arizona

SESSION 2B

Wednesday April 8

Detection, Validation, and Reverse Engineering of Malicious Hardware

Chair: **Hossein Sayadi**, California State University, Long Beach

1:40PM
2B.1

78 **Reference-Free EM Validation Flow for Detecting Triggered Hardware Trojans**
Mahsa Tahghigh and Hassan Salmani
Howard University

2:00PM
2B.2

79 **Reliable Hardware Trojan Detection for RISC-V Processors using Formal Verification and Automation**
Czea Sie Chuah[1], Christian Appold[2], Tim Leinmüller[2]
[1]Technical University of Munich, [2]DENSO AUTOMOTIVE Deutschland GmbH

2:20PM
2B.3

148 **BERT-HIT: A Transformer-Based Approach for Hardware Trojan Detection in Gate-Level Netlists**
Lizi Zhang[1], Navid Tehrani[1], Azadeh Davoodi[2], Rasit Onur Topaloglu[3]
[1]University of Wisconsin, Madison, [2]University of Wisconsin - Madison, [3]Adeia

2:40PM

2B.4

Reverse Engineering RTL Models from DSP Slices in FPGA Netlists

145 *Avinash Hegde Kota[1], Aparajithan Nathamuni-Venkatesan[2], Ranga Vemuri[3], John Emmert[2]*

[1]Digital Design Environments Lab, Dept. of ECE, University of Cincinnati, [2]University of Cincinnati, [3]Univ of Cincinnati

3:00PM

2B.5

131 **Security-Aware Printed-Circuit-Board Routing Based on Deep Reinforcement Learning**

Katherine Shu-Min Li[1], Ching-Han Lai[1], Fang-Chi Wu[1], Sying-Jyan Wang[2]

[1]National Sun Yat-sen University, [2]National Chung Hsing University

SESSION 2C

Wednesday April 8

AI & Machine Learning Acceleration – Architectures and Co-Design

Chair: **Banafsheh Saber Latibari**, University of Arizona

1:40PM
2C.1
7 **Carbon Emission-Based Sustainability Model For Photonic Neural Network Accelerators**
Siqin Liu[1], Avinash Karanth[1], Ahmed Louri[2]
[1]Ohio University, [2]George Washington University

2:00PM
2C.2
38 **FlexGO: A Unified Overlay for General Graph Neural Network Acceleration**
Pramath Balisavira, Rishov Sarkar, Cong Hao
Georgia Institute of Technology

2:20PM
2C.3
44 **Bhasha-Rupantarika: Algorithm-Hardware Co-design approach for Multi-lingual Neural Machine Translation**
Mukul Lokhande[1], Tanushree Dewangan[1], Sharik Mansoori[2], Tejas Chaudhari[3], Akarsh J.[1], Damayanti Lokhande[4], Adam Teman[5], Santosh Vishvakarma[6]
[1]Indian Institute of Technology Indore, [2]Undergraduate, [3]Indian Institute of Technology, Indore, [4]Independent, [5]Bar-Ilan University, [6]IIT Indore

2:40PM
2C.4
58 **TinyQL: A Quantum Machine Learning Framework at Edge for Resource-Constrained IoT Devices**
Maurice Ngouen, Mohammad Rahman, Alexander Perez-Pons, Nagarajan Prabakar
Florida International University

3:00PM

2C.5

Hardware Software Co-Optimization for RISC-V Based High-Performance

167 **Hyperdimensional Computing Architectures**

Priyanka Agarwal[1], Arun M[2], Chandan N S[3], Shrinidhi Rao[2], Madhav Rao[2]

[1]IIIT Bangalore, [2]International Institute of Information Technology-Bangalore, [3]International Institute of Information Technology Bangalore

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SESSION PW1

Thursday April 9

Short Presentation & WIP Session 1

Chair: **Hossein Sayadi**, California State University, Long Beach

9:40AM
PW1.1
166 **Sparsity Aware Pre-processing for Systolic Array Dataflow Acceleration**
Tadikonda Venkata Sai Chaitanya[1], Bhargav D V[2], Madhav Rao[2]
[1]International Insititute of Information Technology-Bangalore, [2]International Institute of Information Technology-Bangalore

9:45AM
PW1.2
Cascaded Reservoir Computing for Temporal Sensor Data: Integrating Physical Dynamics with Echo State Networks
59 *Md Razuan Hossain[1], Imran Fahad[2], Braylen Robinson[2], Sai Swaminathan[2], Hritom Das[3]*
[1]Utah Valley University, [2]The University of Tennessee, Knoxville, [3]Oklahoma State University

9:50AM
PW1.3
30 **VeriRAG: A Retrieval-Augmented Framework for Automated RTL Testability Repair**
Haomin Qi, Yuyang Du, Lihao Zhang, Soung Chang Liew, Kexin Chen, Yining Du
The Chinese University of Hong Kong

9:55AM
PW1.4
9 **Semantic-Guided Test Generation using Fine-Tuned LLMs for Validation of Hardware Accelerators**
Emma Andrews[1], Aruna Jayasena[2], Prabhat Mishra[1]
[1]University of Florida, [2]University of Tennessee

10:00AM

PW1.5

34 **TCAD-Based GGNMOS Digital-Twin for ESD Characterization & Sensitivity Analysis**

Kunaal Pulli[1], Mehrdad Nourani[1], Charvaka Duvvury[2]

[1]The University of Texas at Dallas, [2]iT2 Technologies

10:05AM

PW1.6

53 **HDL-DFGen: A Digital Filter Hardware Description Generation Framework**

Pedro Pereira[1], Sergio Bampi[2], Eduardo Costa[2]

[1]Universidade Federal do Rio Grande do Sul, [2]UFRGS - Federal Univ. of Rio Grande do Sul

10:10AM

PW1.7

61 **Automatic Compact Model Parameter Extraction with an Enhanced Hybrid of Differential Evolution and Nelder-Mead Optimizers**

Fahad Usmani, Zijian Song, Roberto Tinti

Keysight Technologies

10:15AM

PW1.8

89 **AutoSim: A Declarative Framework for Simulator-Agnostic Hardware Verification Automation**

Bhagirath K, Dheeraj Pant, Abhishek Tiwari, Vivek Khaneja

Centre for Development of Advanced Computing

SESSION PW2

Thursday April 9

Short Presentation & WIP Session 2

Chair: **Farah Ferdaus**, Lamar University

9:40AM

PW2.1

FSMVision: Semantic Extraction of Finite State Machines from Diagrams via Multimodal AI

170

Sagor Chandro Bakchy[1], Muhammad Aminul Islam[2], Sazadur Rahman[3], Md Tauhidur Rahman[1]

[1]Florida International University, [2]University of New Haven, [3]University of Central Florida

9:45AM

PW2.2

Multi-Die Concurrent Global Placement with Macro Flipping-aware Wirelength Model for 3D-ICs

111

Anh Phan[1], Cheng-Xun Song[1], Sheng-Tan Huang[1], Shao-Yun Fang[1], Tung-Chieh Chen[2], Kai-Shun Hu[2], Chin-Fang Shen[2]

[1]National Taiwan University Of Science and Technology, [2]Synopsys Taiwan Co., Ltd.,

9:50AM

PW2.3

Modeling Endurance Degradation of VCM-based 1T1R ReRAM Cell for Circuit Simulations

45

Supriya Chakraborty[1], Seyed Hossein Hashemi Shadmehri[2], Thiago Copetti[2], Tobias Gemmeke[2], Leticia Poehls[3]

[1]RWTH Aachen University, [2]RWTH Aachen University, [3]IHP - Leibniz Institute for High Performance Microelectronics, Frankfurt (Oder), Germany

9:55AM

PW2.4

Monolithic 3D Integration for Null Convention Logic (NCL)-Based Asynchronous Circuits

60

Xiameng Zhang[1], Ashiq Sakib[2], Kushal Ponugoti[3], Madhava Sarma Vemuri[1]

[1]University of Washington Bothell, [2]Southern Illinois University Edwardsville, [3]North Dakota State University

10:00AM

PW2.5

Data Augmentation Strategies for Machine Learning-based Compact Modeling of Emerging Devices

107

Diego Ferrer[1], Md Mazharul Islam[2], Wei Pan[3], Juan Mendez Granado[3], Denis Mamaluy[3], Ahmedullah Aziz[4]

[1]The University of Tennessee, Knoxville, [2]The University of Tennessee, [3]Sandia National Laboratory, [4]University of Tennessee, Knoxville

10:05AM

PW2.6

87 **A Compact Gray-Code Quantum Read-only Memory for the NISQ Era**

Hao Yu Lu[1], Yu-Ting Kao[2], Yeong-Jar Chang[2], Chao-Hung Wang[1], Darsen Lu[1]

[1]National Cheng Kung University, [2]Industrial Technology Research Institute

10:10AM

PW2.7

100 **Trusted Memory Access Monitoring (TMAM): Detecting Fine-Grained DDR4 Access Patterns in FPGA Clouds**

Vineet Chadalavada[1], Nahush Tambe[1], Naseeruddin Lodge[1], Dhurva Aklekar[1], fareena saqib[2]

[1]UNC Charlotte, [2]University of North Carolina at Charlotte

10:15AM

PW2.8

132 **Unsupervised Learning Based Hardware Trojan Detection Method for RTL Designs**

Sying-Jyan Wang[1], Hou-Cheng Chen[1], Katherine Shu-Min Li[2]

[1]National Chung Hsing University, [2]National Sun Yat-sen University

10:20AM

PW2.9

28 **Reusing Assertion Properties as Hardware Checkers: Implementation and their Software and Hardware Recovery**

Czea Sie Chuah[1], Christian Appold[2], Tim Leinmueller[2]

[1]Technical University of Munich, [2]DENSO AUTOMOTIVE Deutschland GmbH

SESSION PW3

Thursday April 9

Short Presentation & WIP Session 3

Chair: **Sergiu Mosanu**, University of Virginia

9:40AM
PW3.1
68 **Detecting Hardware Trojans in Quantum Circuits Based on CodeBERT model**
Min-Chao Huang[1], Chin-Wei Tien[2], Sy-Yen Kuo[1]
[1]National Taiwan University, [2]Trend Micro

9:45AM
PW3.2
130 **Unsupervised Detection of Ring-Oscillator Hardware Trojans via Autoencoder Power Analysis**
Oyshi Sarker[1] and Jaya Dofe[2]
[1]California State University Fullerton, [2]California State University

9:50AM
PW3.3
141 **Characterizing On-Chip Variability of Anderson PUF**
Quoc Huy Lieu[1] and Jaya Dofe[2]
[1]California State University Fullerton, [2]California State University

9:55AM

PW3.4

TrackGNN: A Highly Parallelized and Self-Adaptive GNN Accelerator for Track Reconstruction on FPGAs

5

Shuyang Li[1], Hanqing Zhang[2], Ruiqi Chen[3], Bruno da Silva[3], Giorgian Borca-Tasciuc[4], Dantong Yu[5], Cong Hao[1]

[1]Georgia Institute of Technology, [2]Zhejiang University, [3]Vrije Universiteit Brussel, [4]Rensselaer Polytechnic Institute, [5]New Jersey Institute of Technology

10:00AM

PW3.5

Enhanced Hybrid Temporal Computing Using Deterministic Summations for Ultra-Low-Power Accelerators

36

Sachin Sachdeva[1], Jincong Lu[1], Wantong Li[1], Sheldon Tan[2]

[1]University of California, Riverside, [2]University of California at Riverside

10:05AM

PW3.6

POSEIDON: A Posit-Optimized Out-of-Order Processor with Transformer Acceleration for Edge Devices

162

Niranjan Gopal[1], Gaurav Nayak[2], Harshvardhan Mishra[3], Madhav Rao[4]

[1]International Institute of Information Technology Bangalore, [2]IIITB, [3]IIIT-B, [4]International Institute of Information Technology-Bangalore

10:10AM

PW3.7

179 **Real-Time Edge Semantics for Drone Swarms via FPGA Perception and On-Device LLMs**

Zhaoqi Wang, Wade Fortney, Peter Forcha, Yu Feng, Gabriel Bendix, Christophe Bobda

University of Florida

10:15AM

PW3.8

188 **RACFlow: An Evolutionary Framework for Compact Reconfigurable Approximate Circuits**

Bhargav D V and Madhav Rao

International Institute of Information Technology-Bangalore

10:20AM

PW3.9

1 **Active Interposers for High Bandwidth Memory**

Andres Ayes and Eby Friedman

University of Rochester

SESSION 3A

Thursday April 9

Advanced Circuit Modeling and Analysis

Chair: **Rouwaida Kanj**, Synopsys/American University of Beirut

10:45AM

3A.1

19 **Effective Capacitance Modeling Using Graph Neural Networks**

Eren Dogan and Matthew Guthaus

University of California, Santa Cruz

11:05AM

3A.2

Gate-Level Average Power Estimation from RTL Activity with Graph Neural Network

124 *Ssu-Chen Chang[1], Yung-Chih Chen[2], Chun-Yao Wang[3], Jian-Meng Yang[4], Pei-Ying Liu[5]*

[1]National Taiwan University of Science and Technology, [2]National Taiwan University of Science and Technology; Arculus System Co. Ltd., [3]Dept. CS, National Tsing Hua University, [4]Arculus System, [5]MicroIP

11:25AM

3A.3

129 **Multi-Node Timing and Power Estimation with Adapter-Based Transfer Learning**

Luis Humberto Pena Trevino[1], Eric Guerra Ribeiro[2], Lirida Naviner[1], Fady Abouzeid[2], Philippe Roche[2]

[1]Télécom Paris, [2]STMicroelectronics

11:45AM

3A.4

Efficient High-Sigma Yield Analysis based on the Deep Ensemble Framework with

160 **Active learning and Augmentation**

Younghun Park[1], Kang Hun Kim[1], Jun Seo Jung[1], Daehwan Lho[2], Honggyoo Ahn[2], Woncheol Lee[2], Taehoon Kim[2], Juho Kim[1]

[1]Sogang University, [2]SK Hynix Inc.

12:05PM

3A.5

185 **Parasitics-Aware Framework for Integrated OTA Sizing and Layout Synthesis in FinFET Technologies**

Endalk Gebru, Subhadip Ghosh, Ramesh Harjani, Sachin S. Sapatnekar
University of Minnesota

SESSION 3B

Thursday April 9

NN Acceleration & Dataflow Optimization

Chair: **Rasit Topaloglu**, Adeia

10:45AM

10 **3B.1**

Accelerating Machine Learning Applications through Optimized Tensor Decompositions

Emma Andrews and Prabhat Mishra
University of Florida

11:05AM

39 **3B.2**

Harmony: A Hardware-Mapping Co-Exploration Framework for Hybrid CIM-based Vision Transformer Accelerator

Yihang Zuo[1], Zexin Fu[2], Cong Wang[3], Yuchao Wu[4], Jiayi Huang[2], Yuzhe Ma[2]
[1]Arizona State University, [2]The Hong Kong University of Science and Technology (Guangzhou), [3]The Hong Kong University of Science and Technology(Guangzhou), [4]The Hong Kong University of Science and Technology

11:25AM

3B.3

126 **BiKA: Kolmogorov-Arnold-Network-inspired Ultra Lightweight Neural Network Hardware Accelerator**

Yuhao Liu[1], Salim Ullah[2], Akash Kumar[1]

[1]Ruhr University Bochum, [2]Ruhr-Universität Bochum

11:45AM

3B.4

Cross-Layer Co-Optimized LSTM Accelerator for Real-Time Gait Analysis

152 *Mohammad Hasan Ahmadilivani[1], Levent Aksoy[2], Mohammad Eslami[3], Alar Kuusik[2], Jaan Raik[2]*

[1]Tallinn University of Tehnology, [2]Tallinn University of Technology, [3]Department of Computer Systems, Tallinn University of Technology

12:05PM

3B.5

Mixed-Precision Booth Factored Systolic Array Design for Accelerating Neural

156 **Networks**

Sneha Dandekar[1], Bhavana S[2], Madhav Rao[1]

[1]International Institute of Information Technology-Bangalore, [2]International Institute of Information Technology, Bangalore

SESSION 3C

Thursday April 9

Security for AI and AI for Security

Chair: **Ahmedullah Aziz**, The University of Tennessee, Knoxville

10:45AM
3C.1
212 **Cross-Layer Security Through Multi-Level Cell Memories from Hardware Obfuscation to AI Model Protection**
Miran Tobar[1], Hassan Nassar[2], Joerg Henkel[3]
[1]Karlsruhe Institute of Technology, [2]Karlsruher Institut für Technologie, [3]KIT

11:05AM
3C.2
Is Mamba Reliable for Medical Imaging?
213 *Banafsheh Saber Latibari[1], Najmeh Nazari[2], Daniel Brignac[1], Hossein Sayadi[3], Houman Homayoun[4], Abhijit Mahalanobis[1]*
[1]University of Arizona, [2]UC Davis, [3]California State University Long Baech, [4]University of California Davis

11:25AM
3C.3
214 **Leaking at the Edge: EM Side-Channel Input Recovery on Edge TPU**
Simon Pankner, Dennis Gnad, Vincent Meyers, Mehdi Tahoori
Karlsruhe Institute of Technology (KIT)

11:45AM

3C.4

215 **Evolving Landscape of Attacks on AI Hardware and Robust Defenses**

Habibur Rahaman, Sudipta Paria, Atri Chatterjee, SWARUP BHUNIA
University of Florida

12:05PM

3C.5

Fine-Grained Patching via Contention Balancer: A Practical Mitigation Strategy for Spectre Vulnerabilities Using SpecScope Contention Maps

219

Najmeh Nazari[1], Banafsheh Saber Latibari[2], Behnam Omidi[3], Hosein Mohammadi Makrani[1], Fatemeh Movafagh[4], Seyede Elahe Hosseini Imeni[5], Chongzhou Fang[6], Khaled khasawneh[3], Houman Homayoun[1], Hossein Sayadi[7]
[1]UC Davis, [2]University of Arizona, [3]George Mason University, [4]Simon Fraser University, [5]University of California Davis, [6]Rochester Institute of Technology, [7]California State University, Long Beach

SESSION 4A

Thursday April 9

Innovative Design Methodologies and Frameworks

Chair: **Jay Dholakia**, AMD

2:10PM
4A.1
Design for Manufacturing and Assembly for Heterogeneous Integration Using Micro-
94 **Transfer Printing**
Robert Fischbach[1], Ronny Frevert[2], Andreas Krinke[1], Sebastian Wicht[3], Jens Lienig[1]
[1]Dresden University of Technology, [2]X-FAB Dresden GmbH & Co. KG, [3]X-FAB Semiconductor Foundries

2:30PM
4A.2
GRPO with State Mutations: Improving LLM-Based Hardware Test Plan Generation
125 *Dimple Kochar[1], Nathaniel Pinckney[2], Guan-Ting Liu[3], Chia-tung Ho[4], Chenhui Deng[4], Haoxing Ren[2], Brucek Khailany[4]*
[1]Massachusetts Institute of Technology, [2]NVIDIA Corporation, [3]NVIDIA Research, [4]Nvidia

2:50PM

4A.3

Thor: Towards General Directed Circuit Graph Encoder with Sample-Efficient Graph

146 **Contrastive Learning**

Wencheng Zou[1], Yiran Xia[2], Haoyu Wang[3], Pan Li[3], Nan Wu[1]

[1]George Washington University, [2]Hong Kong University of Science and Technology, [3]Georgia Institute of Technology

3:10PM

4A.4

Area-Oriented Threshold Logic Circuit Synthesis Using Negative Weights

138 *Yu-Chuan Yen[1], Fu-Cheng Cai[1], Yi-Ting Li[1], Wuqian Tang[1], Yung-Chih Chen[2], Ihao Chen[3], Chun-Yao Wang[1]*

[1]National Tsing Hua University, [2]National Taiwan University of Science and Technology, [3]Incentia Design Systems Inc.

SESSION 4B

Thursday April 9

Fault, Memory, and Physical Attacks on Hardware Systems

Chair: **Rouwaida Kanj**, Synopsys/American University of Beirut

2:10PM
4B.1
103 **Descrambling the Scrambler: Experimental Extraction of Data Scrambling Keys in COTS NAND Flash**
Matchima Buddhanoy[1], Habib Ur Rahman[1], Aleksandar Milenkovic[2], Sudeep Pasricha[1], Biswajit Ray[1]
[1]Colorado State University, [2]The University of Alabama in Huntsville

2:30PM
4B.2
80 **Characterization of the Stability of DRAM Read Disturbances**
Roberto Capoferri[1], Alessandro Barenghi[2], Luca Breveglieri[1], Khalil Gammoh[3], Niccolò Izzo[3], Gerardo Pelosi[1]
[1]Politecnico di Milano, [2]Politecnico di Milano - DEIB, [3]Micron

2:50PM
4B.3
48 **Power-Off Laser Attack Against Bulk Built-in Current Sensors**
Raphael Viera, No ?Backert, Jean-Max Dutertre
Mines Saint-Etienne

3:10PM

4B.4

164 **An Efficient Memory Cell Flipping Technique Under Covert Channel Attacks**

Prokash Ghosh[1], Sundeep Agrawal[1], Sonali Dulange[1], Subhajit Dutta Chowdhury[2]
[1]AMD Inc, USA, [2]AMD

3:30PM

4B.5

192 **CRISP: Platform-Agnostic Unified Reconfigurable Hardware Security Primitive**

Atri Chatterjee, Sudipta Paria, Aritra Dasgupta, Habibur Rahaman, Baibhab Chatterjee, SWARUP BHUNIA
University of Florida

SESSION 4C

Thursday April 9

Neuromorphic Computing

Chair: **Farah Ferdaus**, Lamar University

2:10PM
4C.1
204 **Enabling Lightweight and Efficient Edge Inference for Identifying Radio Modulation**
Kang Jun Bai[1] and Michelle Jiang[2]
[1]Air Force Research Laboratory, [2]Carnegie Mellon University

2:30PM
4C.2
210 **Robustness Analysis of Neuromorphic Embodied AI Robot for Associative Learning against Adversarial Stickers**
Tianze Liu[1], Kang Jun Bai[2], Hongyu An[1]
[1]Michigan Technological University, [2]Air Force Research Laboratory

2:50PM
4C.3
211 **Heterogeneous Compute-in-Memory Fabrics for Efficient, Scalable Edge Inference and Learning**
Luqi Zheng, Zeshu Wang, Shuting Du, Mufeng Chen, Amir Massah Bavani, Haitong Li
Purdue University

3:10PM

4C.4

202 **S-OPTQ: Rapid Quantization for Spiking Vision Transformers**

Zaidao Mei and Qinru Qiu
Syracuse University

3:30PM

4C.5

Agentic AI for Chip Design Verification: Failure Modes, Metrics, and Coverage Closure

218 *Noah Marosok[1], Marcus Halm[2], Kevin Immanuel Gubbi[2], Mohammadnavid Tarighat[2], Neusha Javidnia[3], Soheil Zibakhsh-Shabgahi[1], Ke Huang[4], Setareh Rafatirad[5], Hossein Sayadi[6], Farinaz Koushanfar[7], Houman Homayoun[5]*
[1]University of California, San Diego, [2]University of California, Davis, [3]UC San Diego, [4]San Diego State University, [5]University of California Davis, [6]California State University, Long Beach, [7]University of California San Diego

SESSION 5A

Friday April 10

Quantum and memory technology and circuits

Chair: **Rasit Topaloglu**, Adeia

8:40AM
5A.1
17 **Delay Register Minimization in RSFQ Circuits**
Chi-En Hsu and Wai-Kei Mak
Department of Computer Science, National Tsing Hua University

9:00AM
5A.2
161 **The Art of Optimizing T-Depth for Quantum Error Correction in Large-Scale Quantum Computing**
Avimita Chatterjee[1], Archisman Ghosh[2], Swaroop Ghosh[1]
[1]Pennsylvania State University, [2]The Pennsylvania State University

9:20AM
5A.3
84 **ULTRARAM: An Emerging Memory Technology for NVM and Low-Power Neuromorphic Systems**
Abhishek Kumar[1], Peter D. Hodgson[2], James Ashforth-Pook[3], Manus Hayne[2], Avirup Dasgupta[4]
[1]University of California Berkeley, [2]Lancaster University, [3]QuInAs Technology Limited, [4]Indian Institute of Technology Roorkee

9:40AM
5A.4
191 **Design and Simulation of Long-Retention Capacitorless 1T-DRAM Using Experimentally Calibrated Process and Device Simulations**
Shao-Han Cheng[1], Chun-Hung Wang[1], Fu-Chang Hsu[2], Yao-Jen Lee[1], Yiming Li[1]
[1]National Yang Ming Chiao Tung University, [2]NEO Semiconductor Inc.

SESSION 5B

Friday April 10

Memory Systems, Approximate Computing, and System-Level Optimization

Chair: **Farah Ferdaus**, Lamar University

8:40AM
5B.1
8 **Multi-Level Cell Memory Driven Efficient Cache Organization**
Binu Christopher[1], Rwicheek Sarker[1], Vivek Bhasi[2], Sumitha George[1]
[1]North Dakota State University, [2]The Pennsylvania State University

9:00AM
5B.2
43 **PEARL: Page Migration for Efficient Hybrid Memory Systems using Adaptive and Lightweight Reinforcement Learning**
Jash Vipul Ratanghayra, Aswathy N S, Hemangee Kapoor
Indian Institute of Technology Guwahati

9:20AM
5B.3
75 **Bit-Flexible Systolic Architecture: Optimizing Processing Elements with Application-Specific Floating-Point Truncation**
Dantu Nandini Devi[1] and Madhav Rao[2]
[1]International Institute of Information Technology Bangalore, [2]International Institute of Information Technology-Bangalore

9:40AM
5B.4
90 **VAE-Enabled Design Space Exploration for Heterogeneous Approximate Matrix Multiplication Accelerators**
Niranjan Gopal[1], Nishith Akula[2], Madhav Rao[3]
[1]International Institute of Information Technology Bangalore, [2]International Institute of Information Technology, Bangalore, [3]International Institute of Information Technology-Bangalore

10:00AM

5B.5

Crossing the Layers and Dotting the Details: Systematic Exploration of Near-Memory Computing

122

Riselda Kodra[1], Rafael Medina Morillas[2], Marina Zapater[3], Giovanni Ansaloni[1], David Atienza[4]

[1]EPFL, [2]ETH Zurich, [3]University of Applied Sciences Western Switzerland (HES-SO), [4]École Polytechnique Fédérale de Lausanne (EPFL)

SESSION 5C

Friday April 10

Neuromorphic and Approximate Computing Hardware for Next-Generation AI

Chair: **Sergiu Mosanu**, University of Virginia

8:40AM
5C.1
BM-HPR Mul: Error Tolerant Hardware Efficient Booth Modified High Precision
150 **Redundant Multiplier**
Chandan N S[1], Yerasi Manoj Reddy[1], Madhav Rao[2]
[1]International Institute of Information Technology Bangalore, [2]International Institute of Information Technology-Bangalore

9:00AM
5C.2
99 **A Low-Power Analog Spiking Neural Network with On-Chip Learning**
Kiruthikan Sithamparanathan and Jeffery Dix
University of Arkansas

9:20AM
5C.3
Hardware-Efficient and Precision-Aware FP16 Approximate Multipliers: A
76 **Probabilistic Approach**
Bindu G Gowda[1] and Madhav Rao[2]
[1]International Institute of Information Technology, Bangalore, [2]International Institute of Information Technology-Bangalore

9:40AM

5C.4

98 **A 4 Transistor eDRAM-Based Content Addressable Memory**

Kayode Adebunmi[1] and Akhilesh Jaiswal[2]

[1]University of Wisconsin Madison, [2]University of Wisconsin-Madison

10:00AM

5C.5

217 **Design Space Exploration of Soft-Error-Tolerant SRAMs for Compute-in-Memory Accelerators**

Jinane Bazzi[1], Rachid Jamil[2], Hicham Masri[2], Ahmad Alayan[2], Rouwaida Kanj[3], Mohammed Fouda[4], Ahmed Eltawil[1]

[1]King Abdullah University of Science and Technology, [2]AUB, [3]Synopsys, [4]Rain Neuromorphics Inc.

SESSION 6A

Friday April 10

Timing and Placement Optimization Techniques

Chair: **Chidhambaranathan Rajamanikkam**, Synopsys

10:30AM
6A.1
23 **Timing-Aware Placement Algorithm for Rapid Single-Flux-Quantum Circuits**
Zhaoting Zhang, Pengming Chen, Zepeng Li, Genggeng Liu
Fuzhou University

10:50AM
6A.2
32 **Hybrid GCN-CNN Framework for Fast Timing-driven Layer Assignment in Global Routing**
Sai Harika Julakanti and Vidya A. Chhabria
Arizona State University

11:10AM

6A.3

Cost-Effective Co-Optimization of SoC Partitioning and Global Chiplet Placement for 2.5D Integration

121

Chou-Yen-Chih Li[1], Chih-Yu Li[1], Yung-Chih Chen[2], Liang-Chia Cheng[3]

[1]National Taiwan University of Science and Technology, [2]National Taiwan University of Science and Technology; Arculus System Co. Ltd., [3]Industrial Technology Research Institute

11:30AM

6A.4

Advanced Techniques for NP3-Boolean Matching: Leveraging Multi-bit Ports and Reverse Engineering to Minimize Search Space

136

Kai-Po Hsu[1], Yi-Ting Li[1], Fu-Cheng Cai[2], Chia-Feng Chien[1], Wuqian Tang[2], Ting-Yu Ku[1], Yu-Chen Cheng[1], Tsung-Han Lai[1], Cheng-Lung Wang[1], Yi-Ting Shen[1], Kuan-Ling Chou[1], Zi-Wei Huang[1], Tao-Chun Huang[1], Tzu-Li Hsu[1], Yung-Chih Chen[3], Shih-Chieh Chang[1], Ting-Chi Wang[1], TingTing Hwang[1], Chun-Yao Wang[1]

[1]National Tsing Hua University, [2]National Tsing Hua Univer, [3]National Taiwan University of Science and Technology

11:50AM

6A.5

163

VHDLBench — a Dataset with Rich Contextual Relationships for Training Custom LLMs

Arpit Sakhreliya and Manoj Franklin

University of Maryland, College park

SESSION 6B

Friday April 10

Security and Robustness of Machine Learning Hardware

Chair: **Farah Ferdaus**, Lamar University

10:30AM
6B.1

157 **Tiny Changes, Big Drops: Unveiling Security Vulnerabilities in ML Accelerators**
Filip Grimsholm[1], Cassandra Westergren[1], Mahdi Fazeli[1], Ahmad Patooghy[2]
[1]Halmstad University, [2]North Carolina A&T State University

10:50AM
6B.2

109 **GBFA: Gradual Bit-Flip Fault Attack on Graph Neural Network Accelerators**
Sanaz Kazemi and Sai Manoj Pudukotai Dinakarrao
George Mason University

11:10AM
6B.3

123 **Ralts: Robust Aggregation for Enhancing Graph Neural Network Resilience on Bit-flip Errors**
Wencheng Zou and Nan Wu
George Washington University

11:30AM

6B.4

A Data-Free Membership Inference Attack on Federated Learning in Hardware

104 **Assurance**

Gijung Lee[1], Wavid Bowman[1], Olivia Dizon-Paradis[1], Reiner Dizon-Paradis[1], Ronald Wilson[2], Damon Woodard[2], Domenic Forte[2]

[1]Florida Institute for National Security, University of Florida, [2]University of Florida

11:50AM

6B.5

35 **CELLM: Confidential and Efficient Lightweight LLM Inference in TEEs**

Hui Feng, Ben Dong, Qian Wang

University of California, Merced

SESSION 6C

Friday April 10

Emerging AI workloads on NPUs

Chair: **Shamik Kundu**, Intel

10:30AM
6C.1
222 **Intelligence Per Watt: A Study of Local Intelligence Efficiency**
Avanika Narayan
Stanford University

10:50AM
6C.2
An Automated Compilation Flow for Efficient GNN Inference on Edge
220 **Heterogeneous Platform**
Haoyang Fan[1], Sameh Gobriel[2], Naveena Padmaraju[2], Chaunte Lacewell[2], Viktor Prasanna[1]
[1]University of Southern California (USC), [2]Intel Labs

11:10AM
6C.3
Uncertainty-Guided Adaptive Model Hopping for Efficient Object Tracking on Edge
221 **Devices**
Divake Kumar[1], Amanda Rios[2], Nilesh Ahuja[2], Omesh Tickoo[2], Amit Trivedi[3]
[1]AEON Lab, AEON Lab, University of Illinois Chicago, [2]Intel Corp., [3]AEON Lab, University of Illinois Chicago

11:30AM
6C.4
223 **FUSE: A Framework for Unified System Evaluation of Accuracy in Edge Inference Accelerators**
Shamik Kundu[1], Arnab Raha[2], Deepak Mathaikutty[2]
[1]Intel Corporation, [2]Intel Labs

11:50AM

6C.5

Closing the Loop: Overcoming the Tool-Feedback Gap in Agentic Hardware Design

216

Mohammadnavid Tarighat[1], Kevin Immanuel Gubbi[1], Neusha Javidnia[2], Noah Marosok[2], Soheil Zibakhsh-shabgahi[2], Marcus Halm[3], Mahdi Pirayesh Shirazi Nejad[3], Setareh Rafatirad[4], Farinaz Koushanfar[5], Houman Homayoun[4]

[1]University of California, Davis, [2]Department of Electrical and Computer Engineering, University of California San Diego, La Jolla, CA 92093, [3]Department of Electrical and Computer Engineering, University of California Davis, Davis, CA 95616, [4]University of California Davis, [5]University of California San Diego

SESSION 7A

Friday April 10

Hyperdimensional, Neuromorphic, and Robust Cognitive Computing Hardware

Chair: **Rouwaida Kanj**, Synopsys/American University of Beirut

12:55PM
7A.1
29 **A Mixed-Signal Neuromorphic Accelerator for Energy Efficient Inference in Event-Based Neural Network Models**
Armin Abdollahi[1], Mehdi Kamal[1], Massoud Pedram[2]
[1]University of Southern California, [2]USC

1:15PM
7A.2
81 **Training Once, Deploy Anywhere: Defect-Robust Memristor Accelerators without Re-Training**
Rejina Maharjan and Chao Lu
Southern Illinois University Carbondale

1:35PM
7A.3
106 **RouteHD: A Routing-Aware FPGA Accelerator for HDC Classification**
Abdullah Sahruri, Alaaddin Goktug Ayar, Sercan Aygun, Martin Margala
University of Louisiana at Lafayette

1:55PM

7A.4

193 **Multi-Stage Compression of Machine Learning Models**

Nahyeon Kim and Prabhat Mishra
University of Florida

2:15PM

7A.5

199 **Early Class Exclusion in Hyperdimensional Computing**

Rémy Duboucheix[1], Mohsen Asghari[1], Sébastien Le Beux[1], Otmane Ait Mohamed[1], Ron Mankarious[2]
[1]Concordia University, [2]PolarSat Inc.

SESSION 7B

Friday April 10

System-Level and Supply-Chain Security for Trusted Computing

Chair: **Banafsheh Saber Latibari**, University of Arizona

12:55PM
7B.1
71 **Security-Quality Scorecard: A Comprehensive Framework for Quantitative Evaluation of Quantitative Evaluation of Hardware-Enforced Boot Chain Security**
Hyunmin Kim
TII

1:15PM
7B.2
97 **Proteus: A Morpheus II Extension for System-Level Moving-Target Defense and Key-Exposure Hardening**
Jeremy Knickerbocker[1], Syed Rafay Hasan[2], Amr Hilal[1], Mohammad Ashiqur Rahman[3]
[1]Tennessee Tech University, [2]Tennessee Tech Univesity, [3]Florida International University

1:35PM
7B.3
172 **A System-Level Design-Space Exploration of Security for Systems-on-Chip**
Abigail Butka, Antonio Hendricks, Christophe Bobda
University of Florida

1:55PM
7B.4
13 **DUA: Detection of Unrecognized Applications Using One-Class SVM in NoC-Based SoCs**
Andrea Galimberti[1], Katsuaki Nakano[2], Rohan Purkait[2], Amlan Ganguly[2], Michael Zuzak[2], Mark Indovina[2], Sai Pudukotai Dinakarrao[3], William Fornaciari[1], Davide Zoni[1]
[1]Politecnico di Milano, [2]Rochester Institute of Technology, [3]George Mason University

2:15PM

7B.5

159 **Shadow Integrity Control (sic)**

Amirreza Hashemi[1], Hans Liljestrand[2], Carlos Chinea Perez[3], Jan-Erik Ekberg[3]

[1]Huawei Technologies/Aalto University, [2]Huawei Technologies, Finland, [3]Huawei Technologies

SESSION 7C

Friday April 10

EdgeAI and Applications

Chair: **Soheil Salehi**, University of Arizona

12:55PM
7C.1
MOTION: ML-Assisted On-Device Low-Latency Motion Recognition
205 *veeramani pugazhenthi[1], Wei-hsiang Chu[2], Junwei Lu[2], Jadyn Miyahira[2], Mahdi Eslamimehr[3], Pratik Satam[1], Rozhin Yasaei[1], Soheil Salehi[4]*
[1]university of arizona, [2]University of California, [3]Quandary Peak Research, [4]Department of Electrical and Computer Engineering, University of Arizona

1:15PM
7C.2
206 **Lightweight Heart Rate Variability Estimation Using PPG Signals**
Ben Brown and Chongzhou Fang
Rochester Institute of Technology

1:35PM
7C.3
207 **A Rapid Pipeline for Training and Deploying ML Models on WeBe Band**
Edwin Kay[1], Asmita Asmita[1], Houman Homayoun[1], Mahdi Eslamimehr[2]
[1]UC Davis, [2]Quandary Peak Research

1:55PM

7C.4

Scalable Security Monitoring on Chiplet-Based Systems

208 *Pooya Aghanoury[1], Sneha Swaroopa[1], Dao Xian Ding[1], Farshad Firouzi[2], Nader Sehatbakhsh[1]*

[1]UCLA, [2]ASU

2:15PM

7C.5

Edge AI-based Anomaly Behavior Analysis for Industrial Control Systems

209 *Zhanglong Yang[1], Qinxuan Shi[1], Yu-Zheng Lin[2], Soheil Salehi[3], Pratik Satam[2], Sicong Shao[1]*

[1]University of North Dakota, [2]University of Arizona, [3]Department of Electrical and Computer Engineering, University of Arizona

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