

FINAL CALL FOR PAPERS

ISQED 2027

28th International Symposium on

QUALITY ELECTRONIC DESIGN



April 14-16, 2027, San Francisco, California, USA

www.isQED.org



AI/ML & Electronic Design, Hardware Security, IoT, Quantum Computing, 3D Integration

The 28th International Symposium on Quality Electronic Design (ISQED'27) is the leading Electronic IC and System Design conference, aimed at bridging the gap among electronic design tools and processes, integrated circuit technologies, processes & manufacturing, to achieve design quality. ISQED is the pioneer and leading international conference dealing with design for manufacturability and quality issues front-to-back. ISQED emphasizes a holistic approach toward electronic design and intends to highlight and accelerate cooperation among the IC & System Design, EDA, Semiconductor Process Technology and Manufacturing communities. ISQED will be held in Hybrid format and spans three days, Wednesday through Friday, in a number of parallel tracks, hosting peer-reviewed technical presentations, several keynote speakers, embedded tutorials, embedded summits, and other informal meetings. Conference proceedings and papers will be published in the IEEE Xplore digital library and indexed by SCOPUS. For any information please contact the publication committee by sending Email to isqedisqed@gmail.com.

PAPERS ARE ACCEPTED IN THE FOLLOWING AREAS

A pioneer and leading multidisciplinary conference, ISQED accepts and promotes papers in the following areas:

EDA Tools and Methodologies & Agentic AI

- ⌘ Agentic AI for Electronic Design and Design Automation (AI): Systems and hardware enabling autonomous, goal-driven AI agents, including cognitive computing, neuromorphic architectures, and secure AI accelerators. Covering design, implementation, and applications in intelligent interaction and cognitive environments.
- ⌘ EDA and physical design tools, processes, methodologies, and flows
- ⌘ Design tools for analysis/ tolerance of variation, aging, and soft-errors
- ⌘ Design and maintenance of hard and soft IP blocks
- ⌘ EDA tools and methodologies for 3D integrations, and advanced packaging
- ⌘ Challenges and solutions of integrating, testing, qualifying and manufacturing IP blocks from multiple vendors
- ⌘ EDA for non-traditional problems such as smart power grid and solar energy
- ⌘ EDA tools and methodologies for 3D integrations, and advanced packaging
- ⌘ Modeling and Simulation of Semiconductor Processes and Devices (TCAD)

Design for Test and Verification

- ⌘ Hardware and software formal-, assertion-, and simulation-based design verification techniques
- ⌘ All areas of DFT, ATE and BIST for digital designs, analog/mixed-signal IC's, SoC's, and memories
- ⌘ Test synthesis and synthesis for testability
- ⌘ Fault diagnosis, IDDQ test, novel test methods, effectiveness of test methods, fault models and ATPG, and DPPM prediction
- ⌘ Design methodologies dealing with the link between testability and manufacturing
- ⌘ SoC/IP testing strategies
- ⌘ Hardware/software co-verification Advanced methodologies, test-benches, and flows (e.g., UVM, HDLs, HVLs)
- ⌘ Formal and semi-formal verification and validation techniques
- ⌘ Safety and security in verification and validation New methods and tools supporting functional safety and security
- ⌘ Self-checking test-benches in analog verification
- ⌘ Any other topics related to design test and verification

Hardware and System Security

- ⌘ Attacks and countermeasures including but not limited to side-channel attacks, reverse engineering, tampering, and Trojans
- ⌘ Hardware-based security primitives including PUFs, TRNGs and ciphers
- ⌘ Security, privacy, trust protocols, and trusted information flow
- ⌘ Ensuring trust using Untrusted tools, IP, models and manufacturing
- ⌘ Ensuring trust using doubtful tools, IP, models and manufacturing
- ⌘ Secure hardware architectures Secure memory systems
- ⌘ Post-quantum security primitives
- ⌘ Security challenges and opportunities of emerging nanoscale devices
- ⌘ IoT and cyber-physical system security
- ⌘ Any other topics related to hardware security

Emerging Device and Process Technologies and Applications

- ⌘ Design, simulation and modeling of emerging technologies
- ⌘ Design, simulation and modeling of emerging non-volatile memory and logic, such as STT-RAM, PC-RAM, R-RAM, and Memristors
- ⌘ Application of emerging devices for storage and computation including but not limited to cognitive, neuromorphic, or quantum computing
- ⌘ Qubit technologies and quantum computing Specialty technologies such as MEMs, NEMs
- ⌘ Novel or emerging solid state nanoelectronic devices and concepts
- ⌘ Design and Technology Co-Optimization
- ⌘ Optimization-based methodologies that address the interaction between design (custom, semi-custom, ASIC, FPGA, RF, memory, etc.)
- ⌘ Advanced-node manufacturing techniques such as multiple patterning, EUV lithography, DSA lithography,
- ⌘ Advanced interconnect (e.g., air gap for local interconnect, Si photonics, etc.).
- ⌘ Modeling, analysis, and optimization of technology implications on performance metrics like power consumption, timing, area, and cost.
- ⌘ Design methods and tools to improve yield and manufacturability.
- ⌘ Any other topics related to emerging device technologies and applications

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Circuit Design, 3D Integration and Advanced Packaging

- ⌘ Low power, high-performance, and robust design of logic, memory, analog, interconnect, RF, programmable logic, and FPGA circuits
- ⌘ Techniques for leakage control, power optimization, and power management
- ⌘ Analog circuit design including but not limited to all-digital PLLs and DLLs, ADC's and DAC's
- ⌘ On-chip process, voltage, temperature, and aging sensors and monitoring
- ⌘ Hardware design for IoT sensors and actuators including digital logic, memory design, wireless communications, energy harvesting, signal processing, and power management
- ⌘ Adaptive and resilient digital circuits and systems
- ⌘ Innovative packaging technologies including 3D IC, 2.5D or interposer, and multi-chip module and their impact on system design
- ⌘ Design techniques, methodologies and flows for vertically integrated circuits/chips
- ⌘ Modeling and mitigation of device interactions for 3D ICs
- ⌘ Design of die-to-die interfaces in 3D/2.5D ICs
- ⌘ Design-for-testability and system-level design issues in 3D/2.5D
- ⌘ Die-package co-design
- ⌘ Any other topics related to circuit design, 3D integration and advanced packaging

Advanced Systems, Architectures & Design Methodologies

- ⌘ Methods and tools aiming at quality of systems including multi-core processors, graphics processors embedded systems, SoC, novel accelerator designs, and heterogeneous architecture designs
- ⌘ System-level trade-off analysis and multi-objective (e.g. yield, power, delay, area, etc.) optimization
- ⌘ System level power and thermal management
- ⌘ Exploration of influence of emerging technologies on the system level design
- ⌘ Cyber-Physical Systems – Design, Methodologies & Tools
- ⌘ System level modeling and simulation to characterize effects of process, voltage, temperature, and aging on power, performance, and reliability
- ⌘ HW/SW co-design, co-simulation, co-optimization, and co-exploration
- ⌘ HW/SW prototyping and emulation on FPGAs
- ⌘ Micro-architectural transformation
- ⌘ System communication architecture
- ⌘ Application driven heterogeneous computing platforms
- ⌘ Network-on-chip design methodologies
- ⌘ Any other topics related to system level design and methodologies

Cognitive Computing Hardware

- ⌘ Neuromorphic computing and non-Von Neumann architectures
- ⌘ Hardware and architecture for neural networks and system-level design for (deep) neural computing Neural network acceleration techniques including GPGPU, FPGA and dedicated ASICs
- ⌘ Safe and secure machine learning Hardware accelerators for Artificial Intelligence Cognitive-inspired computing fundamentals
- ⌘ Cognitive-inspired computing systems
- ⌘ Cognitive-inspired computing with big data
- ⌘ Cognitive-inspired intelligent interaction AI-assisted cognitive computing approaches
- ⌘ Brain analysis for cognitive-inspired computing Internet of cognitive Things
- ⌘ Cognitive environment, sensing and data
- ⌘ Cognitive robots and agents Security issue in cognitive-inspired computing
- ⌘ Test-bed, prototype implementation and applications
- ⌘ Any other topics related to cognitive computing hardware

SUBMISSION OF PAPERS

Paper submissions must be made online through the ISQED conference website at www.isqed.org. Guidelines for preparing and formatting manuscripts are also available on the conference website. Authors are invited to submit original, previously unpublished papers accompanied by an abstract of approximately 200 words. Manuscripts must be at least four (4) pages in length and should preferably not exceed ten (10) pages. A font size of at least 10 points must be used, and manuscripts must conform to the required conference format provided at www.isqed.org. Manuscripts exceeding ten (10) pages and/or using a font size smaller than 10 points may not be reviewed. Manuscripts of fewer than four (4) pages will automatically be considered Work-in-Progress (WIP) papers and will be reviewed accordingly. ISQED follows a blind review process. *Authors must not include their names, affiliations, or any other identifying information in the submitted manuscript or abstract.* Complete contact information for the corresponding author must be entered separately through the online submission system. Manuscripts that identify the name(s) and/or affiliation(s) of the author(s) will be rejected without review. Authors are strongly encouraged to carefully review the final, as-printed appearance of their manuscript before submission to ensure that all text, figures, tables, and references are properly formatted and legible. For questions or assistance with the submission process, please contact isqedisqed@gmail.com.

CALL FOR SPECIAL SESSION PROPOSALS

ISQED'27 is soliciting proposals for special sessions from both academia and industry. The proposed special sessions should aim at offering a complementary experience to the regular sessions and are of general interest to the audience of ISQED. For further information, visit the conference website. All special session proposals should be sent to isqedisqed@gmail.com. Deadline for submission of special session papers is Oct. 25, 2025

WORK IN PROGRESS (WIP) SUBMISSION

Ongoing research projects can be presented at ISQED under the Work in Progress (WIP) category. This provides a unique opportunity to authors to receive early feedback on their current work. Authors of accepted WIP papers would be able to present a poster, as well as a brief oral presentation about their work at ISQED. A short version of the paper will also be included in the conference proceedings.

🔗 Important Deadlines 🔗

FINAL Submission Deadline (Regular, WIP)	Nov. 17 2026
Acceptance Notifications	Jan. 22, 2027
Final Camera-Ready paper	Feb. 17, 2027

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