Call for Papers

ISQED 2025
26th International Symposium on
QUALITY ELECTRONIC DESIGN

April 23-25, 2025 - Hybrid Format
San Francisco, California, USA

isQED
www.isQED.org

IEEE CAS EDS Electron Devices Society acm In-Cooperation sigda

AI/ML & Electronic Design, Hardware Security, IoT, Quantum Computing, 3D Integration

The 26th International Symposium on Quality Electronic Design (ISQED'25) is the leading Electronic IC and System Design conference, aimed at bridging the gap among electronic design tools and processes, integrated circuit technologies, processes & manufacturing, to achieve design quality. ISQED is the pioneer and leading international conference dealing with design for manufacturability and quality issues front-to-back. ISQED emphasizes a holistic approach toward electronic design and intends to highlight and accelerate cooperation among the IC & System Design, EDA, Semiconductor Process Technology and Manufacturing communities. ISQED will be held in Hybrid format and spans three days, Wednesday through Friday, in a number of parallel tracks, hosting peer-reviewed technical presentations, several keynote speakers, embedded tutorials, embedded summits, and other informal meetings. Conference proceedings and papers will be published in the IEEE Xplore digital library and indexed by SCOPUS. For any information please contact the publication committee by sending Email to *isqedisqed@gmail.com*.

Papers are accepted in the following areas

A pioneer and leading multidisciplinary conference, ISQED accepts and promotes papers in the following areas:

Hardware and System Security

- Attacks and countermeasures including but not limited to side-channel attacks, reverse engineering, tampering, and Trojans
- Hardware-based security primitives including PUFs, TRNGs and ciphers
- Security, privacy, trust protocols, and trusted information flow
- Ensuring trust using Untrusted tools, IP, models and manufacturing
- Ensuring trust using doubtful tools, IP, models and manufacturing
- Secure hardware architectures Secure memory systems
- Post-quantum security primitives
- Security challenges and opportunities of emerging nanoscale devices
- IoT and cyber-physical system security
- Any other topics related to hardware security

Electronic Design Automation Tools and Methodologies

- EDA and physical design tools, processes, methodologies, and flows
- Design tools for analysis/ tolerance of variation, aging, and soft-errors
- Design and maintenance of hard and soft IP blocks
- Challenges and solutions of integrating, testing, qualifying and manufacturing IP blocks from multiple vendors
- EDA for non-traditional problems such as smart power grid and solar energy
- EDA tools and methodologies for 3D integrations, and advanced packaging
- Modeling and Simulation of Semiconductor Processes and Devices (TCAD)
- CAD for bio-inspired and neuromorphic systems
- EDA tools, methodologies and applications for Photonics devices, circuit and system design
- EDA for MEMS Any other topics related design automation tools and methodologies

Design for Test and Verification

- Hardware and software formal-, assertion-, and simulation-based design verification techniques
- All areas of DFT, ATE and BIST for digital designs, analog/mixed-signal IC's, SoC's, and memories
- Test synthesis and synthesis for testability
- Fault diagnosis, IDDQ test, novel test methods, effectiveness of test methods, fault models and ATPG, and DPPM prediction
- Design methodologies dealing with the link between testability and manufacturing
- SoC/IP testing strategies
- Hardware/software co-verification Advanced methodologies, test-benches, and flows (e.g., UVM, HDLs, HVLs)
- Formal and semi-formal verification and validation techniques
- Safety and security in verification and validation New methods and tools supporting functional safety and security
- Self-checking test-benches in analog verification
- Any other topics related to design test and verification

Emerging Device and Process Technologies and Applications

- Design, simulation and modeling of emerging technologies
- Design, simulation and modeling of emerging non-volatile memory and logic, such as STT-RAM, PC-RAM, R-RAM, and Memristors
- Application of emerging devices for storage and computation including but not limited to cognitive, neuromorphic, or quantum computing
- Qubit technologies and quantum computing Specialty technologies such as MEMs, NEMs
- Novel or emerging solid state nanoelectronic devices and concepts
- Design and Technology Co-Optimization
- Optimization-based methodologies that address the interaction between design (custom, semi-custom, ASIC, FPGA, RF, memory, etc.)
- Advanced-node manufacturing techniques such as multiple patterning, EUV lithography, DSA lithography,
- Advanced interconnect (e.g., air gap for local interconnect, Si photonics, etc.).
- Modeling, analysis, and optimization of technology implications on performance metrics like power consumption, timing, area, and cost.
- Design methods and tools to improve yield and manufacturability.
- Any other topics related to emerging device technologies and applications

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Circuit Design, 3D Integration and Advanced Packaging

- Low power, high-performance, and robust design of logic, memory, analog, interconnect, RF, programmable logic, and FPGA circuits
- Techniques for leakage control, power optimization, and power management
- Analog circuit design including but not limited to all-digital PLLs and DLLs, ADC's and DAC's
- On-chip process, voltage, temperature, and aging sensors and monitoring
- Hardware design for IoT sensors and actuators including digital logic, memory design, wireless communications, energy harvesting, signal processing, and power management
- Adaptive and resilient digital circuits and systems
- Innovative packaging technologies including 3D IC, 2.5D or interposer, and multi-chip module and their impact on system design
- Design techniques, methodologies and flows for vertically integrated circuits/chips
- Modeling and mitigation of device interactions for 3D ICs
- Design of die-to-die interfaces in 3D/2.5D ICs
- Design-for-testability and system-level design issues in 3D/2.5D
- Die-package co-design
- Any other topics related to circuit design, 3D integration and advanced packaging

System-level Design and Methodologies

- Methods and tools aiming at quality of systems including multi-core processors, graphics processors embedded systems, SoC, novel accelerator designs, and heterogeneous architecture designs
- System-level trade-off analysis and multi-objective (e.g. yield, power, delay, area, etc.) optimization
- System level power and thermal management
- Exploration of influence of emerging technologies on the system level design
- Cyber-Physical Systems – Design, Methodologies & Tools
- System level modeling and simulation to characterize effects of process, voltage, temperature, and aging on power, performance, and reliability
- HW/SW co-design, co-simulation, co-optimization, and co-exploration
- HW/SW prototyping and emulation on FPGAs
- Micro-architectural transformation
- System communication architecture
- Application driven heterogeneous computing platforms
- Network-on-chip design methodologies
- Any other topics related to system level design and methodologies

Cognitive Computing Hardware

- Neuromorphic computing and non-Von Neumann architectures
- Hardware and architecture for neural networks and system-level design for (deep) neural computing Neural network acceleration techniques including GPGPU, FPGA and dedicated ASICs
- Safe and secure machine learning Hardware accelerators for Artificial Intelligence Cognitive-inspired computing fundamentals
- Cognitive-inspired computing systems
- Cognitive-inspired computing with big data
- Cognitive-inspired intelligent interaction AI-assisted cognitive computing approaches
- Brain analysis for cognitive-inspired computing Internet of cognitive Things
- Cognitive environment, sensing and data
- Cognitive robots and agents Security issue in cognitive-inspired computing
- Test-bed, prototype implementation and applications
- Any other topics related to cognitive computing hardware

Submission of Papers

Paper submission must be done on-line through the conference web site: www.isqed.org. The guidelines for the final paper format are provided on the conference web site. Authors should submit original, unpublished papers along with an abstract of about 200 words. The manuscripts should at least four (4) pages long but not preferably exceed eight (8) pages, should not use smaller than 10pt font size, and must be consistent with the format provided in the conference website: www.isqed.org. The manuscripts longer than 8 pages and/or written in less than 10pt font sizes might not be reviewed. To permit a blind review, do not include name(s) or affiliation(s) of the author(s) on the manuscript and abstract. The complete contact author information needs to be entered separately. The manuscripts identifying the name and/or affiliations of the authors in the submitted manuscript will be rejected without review. Please check the as-printed appearance of your paper before sending your paper. In case of any

Call for Special Session Proposals

ISQED'24 is soliciting proposals for special sessions from both academia and industry. The proposed special sessions should aim at offering a complementary experience to the regular sessions and are of general interest to the audience of ISQED. For further information, visit the conference website. All special session proposals should be sent to to *isqedisqed@gmail.com.* Deadline for submission of special session papers is Oct. 15, 2024

Work in Progress (WIP) Submission

Ongoing research projects can be presented at ISQED under the Work in Progress (WIP) category. This provides a unique opportunity to authors to receive early feedback on their current work. Authors of accepted WIP papers would be able to present a poster, as well as a brief oral presentation about their work at ISQED. A short version of the paper will also be included in the conference proceedings.

Special Issue Journals & Selection Process

Selected papers from ISQED'25 will be invited for submission in the special issues of a number of journals. List of journals will be announced later. The selection process for these special issues will take place after the conference is completed and will be based on reviewer feedback and the quality of the conference presentation.

Important Deadlines

Extended Submission Deadline (Regular, WIP)	**Oct. 25, 2024**
Acceptance Notifications	Jan. 15, 2025
Final Camera-Ready paper	Feb. 17, 2025

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