Final Program

AI/ML & Electronic Design, Security, IoT, Autonomous Vehicles, Quantum Computing

ISQED

2025
26th International Symposium on

QUALITY ELECTRONIC DESIGN

April 23-25, 2025
Seven Hills Conference Center
San Francisco State University
San Francisco, CA US

25 YEARS ANNIVERSARY

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International Society for Quality Electronic Design

WELCOME TO ISQED'25

It is with great pleasure that we welcome you to the 26th International Symposium on Quality Electronic Design (ISQED 2025). Building on last year's celebration of 25 years of innovation and leadership, this year's symposium continues our commitment to advancing the principles of Quality Electronic Design (QED) in an ever-evolving technological landscape.

In the spirit of accessibility and engagement, ISQED 2025 continues with a hybrid conference format—offering the richness of in-person interactions at the Seven Hills Conference Center at San Francisco State University, while also providing virtual access to participants worldwide. This blended approach allows us to connect a truly global community of innovators, researchers, and industry leaders.

ISQED has long stood at the forefront of driving progress in semiconductor design and electronic systems. This year's program builds on that legacy, presenting a dynamic agenda that includes keynote speeches, expert panels, hands-on tutorials, and more than 100 rigorously reviewed technical papers—all reflecting our unwavering focus on quality and innovation.
This year's highlights include:

Keynote Speakers
Dr. Haoxing (Mark) Ren, Nvidia
AI for Chip Design

Prof. Nael Abu-Ghazaleh, University of California, Riverside
Security and Privacy for Extended Reality Systems: Attacks and Threat Models

Embedded Tutorials
Dr. Zuguo (Joe) Wu, Intel
Scalable and Reliable On-Package I/O: UCIe Innovations and Best Practices

Dr. Juthika Basak, AMD
Silicon Photonics for High Performance Computing

Panel Discussion
Cryogenic Electronics: Powering the Next Frontier in AI and Computing

We are proud to once again receive technical sponsorship from two premier IEEE societies—the Electron Devices Society and the Circuits and Systems Society—as well as the continued collaboration with ACM/SigDA. As always, ISQED proceedings will be published in the IEEE Xplore digital library and indexed in Scopus, ensuring that the knowledge shared here reaches a global scholarly audience.

Our 2025 program highlights transformative areas such as Artificial Intelligence and Machine Learning, Autonomous Systems, IoT, Cybersecurity, and Quantum Computing. Attendees can expect deep insights and forward-looking discussions across four parallel tracks, showcasing work at the intersection of theory and real-world application in circuits, systems, verification, and design automation.

This year's conference runs from April 23–25, Pacific Daylight Time (PDT), and every session—from plenaries to tutorials—will be accessible both on-site and online, reinforcing our dedication to inclusivity and knowledge-sharing across borders.
We extend our sincere thanks to our sponsors, Innovotek and Silicon Valley Polytechnic Institute, whose generous support continues to empower our mission and expand the impact of ISQED.

Welcome to ISQED 2025—where innovation, collaboration, and excellence come together to shape the future of quality electronic design.

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Virginia Tech

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California State University, Long Beach

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Publication Chair
Paul Wesling
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Silicon Valley Polytechnic Institute

ISQED'25 Best Papers

1C.1

AutoFlows: Inferring Message Flows From System Communication Traces

Bardia Nadimi, Hao Zheng

Department of Computer Science and Engineering
University of South Florida

2A.2

VRank: Enhancing Verilog Code Generation from Large Language Models via Self-Consistencyand Simulation Schemes

Zhuorui Zhao[1], Ruidi Qiu[1], Ing-Chao Lin[2], Grace Li Zhang[3], Bing Li[4], Ulf Schlichtmann[1]

[1]Chair of Electronic Design Automation, Technical University of Munich (TUM), Munich, Germany
[2]Computer Architecture and IC Design, National Cheng Kung University
[3]Hardware for Artificial Intelligence Group, Technical University of Darmstadt
[4]Research Group of Digital Integrated Systems, University of Siegen

Authors of best papers are acknowledged during the morning plenary session on Wednesday April 23.
ISQED'25 best papers are sponsored by **Silicon Valley Polytechnic Institute**.

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Kang Jun Bai - Air Force Research Laboratory
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Deliang Fan - Arizona State University
Haowen Fang - Synopsys
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Geng Yuan - University of Georgia

Design Test and Verification (DTV)

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Arnaud Virazel - LIRMM
Heng Wu - Peking University
zhichao Zhang - Intel

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Shih-Hsu Huang - Chung Yuan Christian University
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Sheikh Ariful Islam - University of Texas Rio Grande Valley
Anand Iyer - Synopsys
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System-level Design and Methodologies (SDM)

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GENERAL INFORMATION
ISQED'25

April 23-25, 2025
Seven Hills Conference Center
San Francisco State University

AWARDS & RECOGNITIONS

Wednesday April 23, 8:40 AM - 9:00 AM
Track A - Nob Hill Room

Best Paper Awards

Recipients of the ISQED'25 Best Paper Awards will be recognized in this segment of the program. The best papers are shown in Page 2 of this document.

Keynotes

Keynote 1P.1

Wednesday, April 23, 9:00 AM - 9:35 AM

AI for Chip Design: Unlocking New Frontiers in Automation and Scaling

Dr. Haoxing (Mark) Ren
Nvidia

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Keynote 2P.1

Thursday, April 24, 9:00 AM - 9:35 AM

Security and Privacy for Extended Reality Systems: Attacks and threat models

Prof. Nael Abu-Ghazaleh
UC Riverside

Panel Discussion

Wednesday, April 23, 3:15 PM - 4:45 PM
Track A - Nob Hill Room

Cryogenic Electronics: Powering the Next Frontier in AI and Computing

As we push the limits of performance in computing, sensing, and quantum technologies, cryogenic electronics has emerged as a trailblazing frontier in modern engineering. This panel will dive into the rapidly evolving field of electronics designed to operate at ultra-low temperatures, where new physics and unprecedented efficiencies become possible. Experts from across the field will share insights on groundbreaking innovations that exploit the unique properties of superconductors, cryogenic memory, and quantum devices to unlock new levels of speed, energy efficiency, and precision. From enabling scalable quantum processors to advancing ultra-sensitive sensors for space and science, cryogenic electronics holds transformative potential across various industries. Join us for an inspiring discussion on the latest breakthroughs, key challenges, and the future directions of cryogenic technology. This is a rare opportunity to gain a deep understanding of the innovations that could redefine computing, data processing, and sensing in the age of extreme electronics.

Panelists:
Dr. Patricia Gonzalez - Lawrence Berkeley National Lab
Dr. James Tandon - cassia.AI
Dr. Hiu-Yung Wong - San Jose State University

Modedrator & Chair:
Dr. Ahmedullah Aziz - University of Tennessee Knoxville

Embedded Tutorials

Chair & Moderators:
Zhen Zhou - Intel (Chair)

Track A - Nob Hill Room

Tutorial 1

Wednesday, April 23, 12:25 PM -1:25 PM

Scalable and Reliable On-Package I/O: UCIe Innovations and Best Practices

Dr. Zuguo (Joe) Wu
Intel

.....

Tutorial 2

Thursday April 24, 1:05 PM -2:05 PM

Optical Transceivers Enabling High Performance Hardware Infrastructure for AI applications

Dr. Juthika Basak
AMD

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TECHNICAL SESSIONS

There are a total of 23 paper sessions held on Wednesday to Friday. Technical sessions are held in the format of three parallel tracks **A, B, C** located respectively in Nob Hill Room, Russian Hill Room, and Mt. Davidson room.

ON-SITE REGISTRATION

Tentative time schedule of on-site registration is as follows:

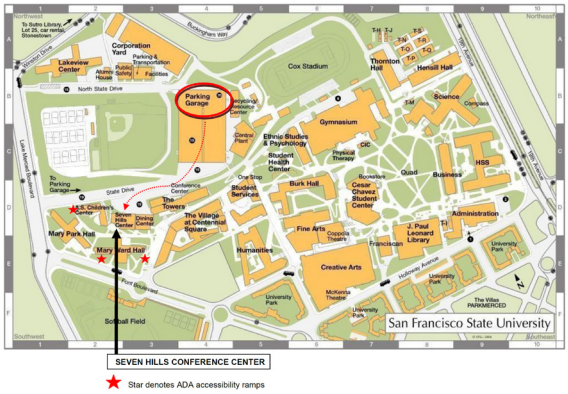
Wednesday, April 23, 8:00 AM - 2:00 PM
Thursday , April 24, 8:00 AM -12:00 PM

Registration desk location will be at the conference center lobby.

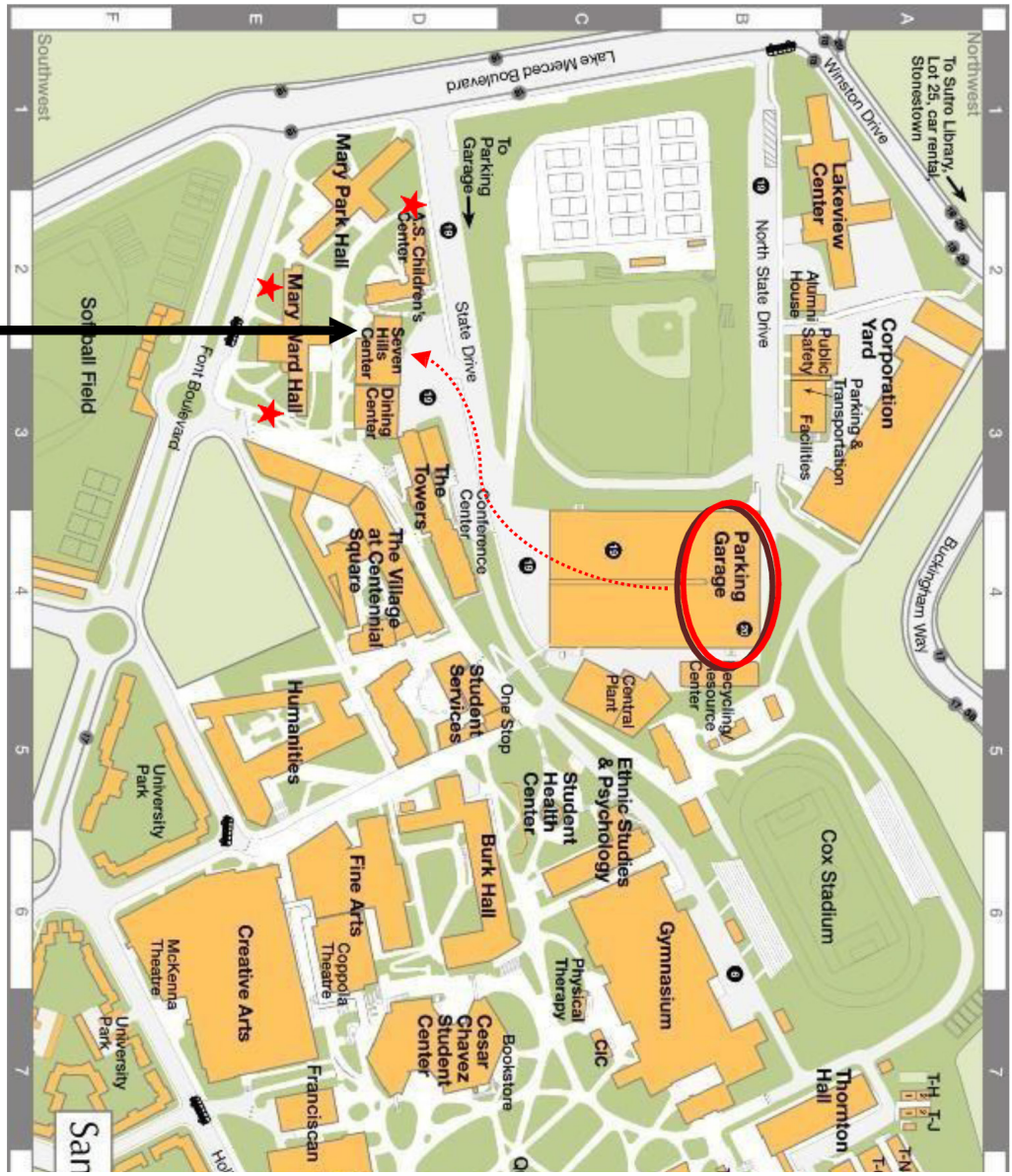
Seven Hills Conference Center

ISQED'25 conference will be held in Seven Hills Conference Center, located in San Francisco State University, 800 Font Blvd, San Francisco, CA 94132.

If you are using navigator the best address to use is: 796 state drive, San Francisco, CA 94132. (Note: make sure to use Google Maps app) At the end of State Drive is the Public Parking Lot ("Lot 20"). Parking is $6.25 for less than 2 hours, and $10 for 2+ hours. Pay stations on each floor accept $1, $5 and $10 bills as well as credit/debit cards. Be advised, pay stations do not provide change. Please have exact amount. From the garage, Seven Hills' entrance can be accessed from State Drive by walking Southwest towards the A.S. Children's Center and taking the staircase beside it up one flight. Wheelchair access: go past the A.S. Children's Center and take a left onto the path. Follow to the entrance to the Seven Hills Conference Center.



UNIVERSITY MAP & CONFERENCE CENTER LOCATION+



WEDNESDAY APRIL 23

	Plenary Session 1: (Track A- Nob Hill Room)		
8:40am–9:00am	**Introduction, Committee Recognitions, Best Paper Awards**		
9:00am-9:35am	**Keynote:** **AI for Chip Design: Unlocking New Frontiers in Automation and Scaling** **Dr. Haoxing (Mark) Ren - Nvidia**		
9:35am–10:10am			
10:10am–10:20am	**Break**		
10:20am–11:40am	**Session 1A (Nob Hill Room)** **Innovations in In-Memory Computing for AI and High-Performance Hardware**	**Session 1B (Russian Hill Room)** **Security Primitives in Modern Designs**	**Session 1C (Mt. Davidson Room)** **Design Verification and High-Speed Memory Testing**
11:40am-12:25pm	**Lunch Break**		
12:25pm-13:25am	**Embedded Tutorial 1 (Track A)** **Scalable and Reliable On-Package I/O: UCIe Innovations and Best Practices** *Presenter:* Zuguo (Joe) Wu - Intel		
13:25pm-13:30pm	**Break**		
13:30pm-15:10pm	**Session 2A (Nob Hill Room)** **Generative AI and its Application to Design Automation**	**Session 2B (Russian Hill Room)** **Security-aware Design Flow for Integeretaed Circuits**	**Session 2C (Mt. Davidson Room)** **Efficient Hardware Architectures for AI and Approximate Computing**
15:10pm-15:15pm	**Break**		
15:15pm-16:45pm	**Panel Discussion - (Track A - Nob Hill Room)** **Cryogenic Electronics: Powering the Next Frontier in AI and Computing**		

THURSDAY APRIL 24

	Plenary Session 2: (Track A - Nob Hill Room)		
8:45am–9:00am	**Welcome**		
9:00am–9:35am	**Keynote:** **Security and Privacy for Extended Reality Systems: Attacks and threat models** **Prof. Nael Abu-Ghazaleh - University of California, Riverside**		
9:35am–9:40am	**Break**		
9:40am-10:35am	**Session PW1 (Nob Hill Room, Track A)** **Short Presentation & WIP Session 1**	**Session PW2 (Russian Hill Room, Track B)** **Short Presentation & WIP Session 2**	**Session PW3 (Mt. Davidson Room, Track C)** **Short Presentation & WIP Session 3**
10:35am-10:45am	**Break**		
10:45am–12:25pm	**Session 3A (Nob Hill Room)** **Simulation and Analysis in VLSI Design**	**Session 3B (Russian Hill Room)** **Recent Trends in Cognitive Computing Hardware**	**Session 3C (Mt. Davidson Room)** **Neuromorphic Computing for Next-gen Machine Intelligence**
12:25pm-13:05	**Lunch Break**		
13:05pm-14:05pm	**Embedded Tutorial 2 (Track A - Nob Hill Room)** **Optical Transceivers Enabling High Performance Hardware Infrastructure for AI applications** *Presenter:* Juthika Basak - AMD		
14:05pm-14:10pm	**Break**		
14:10pm-15:50pm	**Session 4A (Nob Hill Room)** **VLSI Physical Design Methodologies**	**Session 4B (Russian Hill Room)** **Security Evaluation in Complex Designs**	**Session 4C (Mt. Davidson Room)** **Generative AI on Edge**

FRIDAY APRIL 25

9:00am-10:40am	**Session 5A** (Nob Hill Room) Memristive and Charge-Trap Devices for Next-Gen Computing	**Session 5B** (Russian Hill Room) AI-Driven Embedded Computing and Power-Aware System Design	**Session 5C** (Mt. Davidson Room) Design Innovation and Accelaration in the Nanometer Era
10:40am-10:45am	Break		
10:45am–12:05pm	**Session 6A** (Nob Hill Room) Advances in Quantum Computing: Security, Optimization, and AI Integration	**Session 6B** (Russian Hill Room) Advanced Signal Processing and AI Acceleration	**Session 6C** (Mt. Davidson Room) Intelligent and Secure Computing for Next-Gen Systems
12:25pm-12:55	Lunch Break		
12:55pm-14:55pm		**Session 7B** (Russian Hill Room) Optimizing Memory, Power, and Computation for Next-Gen Systems	**Session 7C** (Mt. Davidson Room) Hardware Techniques in Quantum Computing Security

Wednesday April 23

9:00 AM - 9:35 AM

Room: Nob Hill

AI for Chip Design: Unlocking New Frontiers in Automation and Scaling

Dr. Haoxing (Mark) Ren

Director of Design Automation Research - Nvidia

The history of EDA is fundamentally a story of two parallel trends: increasing automation of manual design tasks and the scaling of these automation techniques to handle ever-larger design complexities. Today, with generative AI and accelerated computing, we are entering a new phase that promises to dramatically advance both fronts. In this talk, I will explore how these technologies can drive the next wave of innovation in EDA. While current commercial offerings in AI for chip design have shown promising progress, the path ahead holds even greater opportunities for innovation and impact. I will present examples from physical and logic design to illustrate how generative AI and GPU-accelerated computing can further enhance automation and enable greater scaling. Specifically, I will cover our recent work on LLM-based gate sizing, synthetic data generation for RTL design, model merging for domain-adapted LLMs, and agent-based RTL coding and debugging. Together, these developments underscore the transformative potential of generative AI and accelerated computing to automate more tasks and scale chip design workflows like never before.

About Haoxing (Mark) Ren

Haoxing (Mark) Ren is the Director of Design Automation Research at NVIDIA, focusing on leveraging machine learning and GPU-accelerated tools to enhance chip design quality and productivity. He has over 25 years of industrial EDA research and development experience at IBM and NVIDIA. He holds over thirty patents and has co-authored over 100 papers and books, including a book on ML for EDA and several book chapters in EDA. He received several prestigious awards for his work, including the IBM Corporate Award and best paper awards at ISPD, DAC, TCAD, MLCAD and LAD. He serves in the organization and steering committees of international conferences such as ICCAD and ISPD and as the conference chair at ICLAD. He holds Bachelor's and Master's degrees from Shanghai Jiao Tong University and Rensselaer Polytechnic Institute, respectively, and earned his PhD from the University of Texas at Austin. He is a Fellow of the IEEE.

ISQED Keynote 2P.1

Thursday April 24

9:00 AM - 9:35 AM

Room: Nob Hill

Security and Privacy for Extended Reality Systems: Attacks and threat models

Dr. Nael Abu-Ghazaleh

Professor in the CSE department, UC Riverside

AR/VR devices promise a new era of immersive computing, where our everyday experience is augmented with helpful information (Augmented Reality), or where we are immersed in fully virtual worlds (Virtual Reality). These systems fuse the physical world, and the virtual world, through computing resources to provide these immersive experiences rendered on the user's headset. As a result, it allows new opportunities for attackers to compromise the security and privacy of users, that are not well understood. Towards understanding the security and privacy challenges in these systems, this talk presents a number of recent attacks we developed on AR/VR systems. One threat model exploits the shared computing resources used by multiple applications on a headset to extract information through side channels; we show attacks that spy on user activity or compromise privacy. Another threat model exploits the shared state among multiple users in a multi-user application, allowing malicious users to inject compromised information or to recover information they are not allowed to access. Other threat models include those that interfere with applications and cause the virtual model to become out of sync with the physical world, causing user motion sickness or bypassing safety guardrails. I will conclude with discussion potential defenses and ways to build more security AR/VR experiences.

About Nael Abu-Ghazaleh

Nael Abu-Ghazaleh is a Professor in the Computer Science and Engineering as well as the Electrical and Computer Engineering Departments at the University of California, Riverside. His research is in architecture and system security, high-performance computing, and systems and security for Machine Learning. He has published over 250 papers in these areas, several of which have been recognized with best paper awards or nominations. His offensive security research has resulted in the discovery of several new attacks on CPUs and GPUs that have been disclosed to companies including Intel, AMD, ARM, Apple, Microsoft, Google, and Nvidia, and resulted in patches and modifications to products, and coverage from technical news outlets. He is a member of the Micro Hall of Fame, an ACM distinguished member, and an IEEE distinguished speaker.

Wednesday April 23

3:25 PM–4:55 PM

Room: Nob Hill

Cryogenic Electronics: Powering the Next Frontier in AI and Computing

Panelists:

Dr. Patricia Gonzalez - Lawrence Berkeley National Lab

Dr. James Tandon - cassia.AI

Dr. Hiu-Yung Wong - San Jose State University

Modedrator/Chair:

Dr. Ahmedullah Aziz - University of Tennessee Knoxville

Summary:

As we push the limits of performance in computing, sensing, and quantum technologies, cryogenic electronics has emerged as a trailblazing frontier in modern engineering. This panel will dive into the rapidly evolving field of electronics designed to operate at ultra-low temperatures, where new physics and unprecedented efficiencies become possible. Experts from across the field will share insights on groundbreaking innovations that exploit the unique properties of superconductors, cryogenic memory, and quantum devices to unlock new levels of speed, energy efficiency, and precision. From enabling scalable quantum processors to advancing ultra-sensitive sensors for space and science, cryogenic electronics holds transformative potential across various industries. Join us for an inspiring discussion on the latest breakthroughs, key challenges, and the future directions of cryogenic technology. This is a rare opportunity to gain a deep understanding of the innovations that could redefine computing, data processing, and sensing in the age of extreme electronics.

Wednesday April 23

12:25 AM - 1:25 PM

Nob Hill Room

Scalable and Reliable On-Package I/O: UCIe Innovations and Best Practices

Dr. Zuguo (Joe) Wu

Intel

Summary:

The transition from traditional System On Chip (SOC) designs to chiplet-based architectures marks a significant evolution in semiconductor technology. This presentation will explore the Universal Chiplet Interconnect Express (UCIe), an open standard that ensures seamless chiplet interoperability within a package. We will delve into the critical innovations of UCIe, highlighting its electrical characteristics, 2D/2.5D/3D packaging, and energy-efficient design that collectively achieve a tenfold reduction in power consumption compared to conventional off-package I/O. A key focus will be on the reliability of densely packed UCIe links, examining the considerations of consistent and error-free data transmission, even at elevated data rates.

About Zuguo (Joe) Wu

Zuoguo Wu is a Senior Principal Engineer at Intel, where he manages an I/O circuits and architecture team working on the latest interfaces. He currently serves as the UCIe Consortium Electrical Working Group Co-Chair. He is a principal author of the UCIe spec and defined its PHY architecture and circuit and link analysis. He is also a key contributor to every generation of the PCIe spec since 3.0. He holds 147 patents worldwide and has published over 50 external and Intel-internal papers. He earned a PhD in electrical engineering from Texas A&M University.

Thursday April 24

1:05 PM - 2:05 PM

Nob Hill Room

Optical Transceivers Enabling High Performance Hardware Infrastructure for AI applications

Dr. Juthika Basak

AMD

Summary:

In recent years, Large Language Models (LLMs) have played a significant role in advancing Generative Artificial Intelligence (Gen AI). The amount of compute needed (in petaFLOPs) to support such LLMs has grown at an exorbitant rate of approximately 750x every 2 years. However, interconnect, DRAM, and hardware bandwidth have not progressed at the same rate, prompting the semiconductor industry to explore disruptive technologies. Optical interconnects, which have become widespread in long haul and metro haul network applications, offer a promising solution. The need for cost-efficient solutions has also hastened adoption of silicon photonics transceivers, in turn driving design and manufacturing innovations in this domain. Silicon Photonics Integrated Circuits (PICs) also lends itself well to the advanced packaging schemes, such as hybrid bonding to the associated analog circuits, viz. drivers and Transimpedance Amplifiers (TIAs). This results in signal integrity interconnects in compact form-factors. This tutorial delves into the fundamentals of optical transceivers, exploring the challenges and opportunities associated with incorporating optics into AI-centric hardware infrastructure.

About Juthika Basak

Juthika Basak is a Fellow at Advanced Micro Devices (AMD) working on cutting edge of Photonics Technologies for improving interconnect bandwidth and increasing compute capacities. Prior to AMD, Juthika worked at Nokia, architecting and leading its new generation of CSTAR (Coherent Silicon Transmitter and Receiver) Trademark product line. She also managed the Advanced Packaging technology development team, delivering multiple generations of coherent products for long haul networks. Juthika also worked at Finisar (acquired by II-VI Corporation and further renamed as Coherent), designing pluggable transceivers for long haul interconnect applications. Leading up to her work on transceiver design, she spent several years at Intel Corporation and Infinera Corporation, working on silicon and III-V photonics technologies, respectively. She completed her B. Tech. in Engineering Physics from the Indian Institute of Technology, Bombay and her M.S. and Ph.D. in Electrical Engineering from University of California, Los Angeles.

ISQED 2025: Program

SESSION 1A

Wednesday April 23

Innovations in In-Memory Computing for AI and High-Performance Hardware

Chair: **Ahmedullah Aziz**, The University of Tennessee, Knoxville

10:15AM
1A.1
In-Memory Template Matching with Approximated PCC Computation Leveraging Memristive System
Sree Nirmillo Biswash Tushar[1], Sk Hasibul Alam[1], Graham Buchanan[1], Rocco Febbo[1], Hritom Das[2], Garrett Rose[1]
[1]University of Tennessee, Knoxville, [2]Oklahoma State University

10:35AM
1A.2
An Error-resilient Compute-in-memory 3D FPCA Architecture for High-performance Floating-point Operations
Hasita Veluri and Dilip Vasudevan
Lawrence Berkeley National Laboratory

10:55AM
1A.3
HIDE: A Hyperdimensional In-DRAM Encoder for Fast and Energy-Efficient Classification
Ahmed Mamdouh and Dayane Reis
University of South Florida

SESSION 1B

Wednesday April 23

Security Primitives in Modern Designs

Chair: **Hossein Sayadi**, California State University, Long Beach

10:15AM
1B.1
XORed Carry Chain Ring Oscillator Factored True Random Number Generator
Kanish R[1] and Madhav Rao[2]
[1]International Institute of Information Technology Bangalore, [2]International Institute of Information Technology-Bangalore

10:35AM
1B.2
Non-Homogeneous Composite Karatsuba Multipliers Factored Hardware-Efficient ECDSA Generation and Verification Accelerator Units
Pruthvi Parate[1], Alwin Shaju[1], Sanampudi Gopala Krishna Reddy[1], Vasanthi D R[1], Madhav Rao[2]
[1]International Institute of Information Technology Bangalore, [2]International Institute of Information Technology-Bangalore

10:55AM
1B.3
Device Boot-up Security Restoration with Post-Quantum Split-key KEM
Joonas Ahola, Jan-Erik Ekberg, Sampo Sovio
Huawei Technologies Oy

11:15AM
1B.4
Quantum Data Breach: Reusing Training Dataset by Untrusted Quantum Clouds
Suryansh Upadhyay[1] and Swaroop Ghosh[2]
[1]Penn State University, [2]Pennsylvania State University

11:35AM

1B.5

RollGuard: Defending RPC Manipulation Attacks in Optimistic Rollups with Graph ML

Alvi Ataur Khalil and Mohammad Ashiqur Rahman
Florida International University

SESSION 1C

Wednesday April 23

Design Verification and High-Speed Memory Testing

Chair: **Chidhambaranathan Rajamanikkam**, Synopsys Inc.

10:15AM
1C.1
AutoFlows: Inferring Message Flows From System Communication Traces
Bardia Nadimi and Hao Zheng
University of South Florida

10:35AM
1C.2
Automated Verilog Assertion Generation Using Fine-Tuned LLMs with Subtask-Specific Iterative Prompting
Mohammad Shahidzadeh[1], Behnam Ghavami[2], Steve Wilton[3], Lesley Shannon[1]
[1]Simon Fraser University, [2]Advanced Micro Devices (AMD), [3]University of British Columbia

10:55AM
1C.3
Leveraging DDR5 RCDs for High-Speed DDR5 Protocol Analysis: A Novel Approach to RDIMM Testing
Xinran Li
Professional

11:15AM
1C.4
Formal Verification of a Custom Compiler for a Fully Homomorphic Encryption Accelerator
Zhenkun Yang[1], Suvadeep Banerjee[2], Jeremy Casas[1], Jin Yang[1]
[1]Intel Corporation, [2]Intel Labs, Intel

SESSION 2A

Wednesday April 23

Generative AI and its Application to Design Automation

Chair: **Chidhambaranathan Rajamanikkam**, Synopsys Inc.

1:40PM
2A.1
EDA-Debugger: An LLM-based Framework for Automated EDA Runtime Issue Resolution
Junyan Li[1], Sam-Zaak Wong[2], Gwok-Waa Wan[2], Xi Wang[1], Yang Jun[3]
[1]Southeast University, [2]NCTIEDA, [3]

2:00PM
2A.2
VRank: Enhancing Verilog Code Generation from Large Language Models via Self-Consistency
Zhuorui Zhao[1], Ruidi Qiu[1], Ing-Chao Lin[2], Grace Li Zhang[3], Bing Li[4], Ulf Schlichtmann[1]
[1]Technical University of Munich, [2]National Cheng Kung University, [3]TU Darmstadt, [4]University of Siegen

2:20PM
2A.3
Paradigm-Based Automatic HDL Code Generation Using LLMs
Wenhao Sun[1], Bing Li[2], Grace Li Zhang[3], Xunzhao Yin[4], Cheng Zhuo[4], Ulf Schlichtmann[1]
[1]Technical University of Munich, [2]University of Siegen, [3]TU Darmstadt, [4]Zhejiang University

2:40PM
2A.4
Toward Automated Potential Primary Asset Identification in Verilog Designs
Subroto Nath and Benjamin Tan
University of Calgary

SESSION 2B

Wednesday April 23

Security-aware Design Flow for Integrated Circuits

Chair: **Tasnuva Farheen**, Louisiana State University

1:40PM
2B.1
FlexGuard: Dynamic Scoring & Stochastic Routing for Balanced Security-Performance in 3D NoCs
Mahdi Hasanzadeh[1], Ebad Taheri[2], Jason Green[1], Abdolhossein Sarrafzadeh[1], Ahmad Patooghy[1]
[1]North Carolina A & T State University, [2]Independent Researcher

2:00PM
2B.2
REDACTOR: eFPGA Redaction for DNN Accelerator Security
Yazan Baddour, Ava Hedayatipour, Amin Rezaei
California State University, Long Beach

2:20PM
2B.3
Power and Area-Efficient ECC Processor with Sequential Recursive Polynomial Multiplier Implementation
Pruthvi Parate[1], Alwin Shaju[1], Vasanthi D R[1], Madhav Rao[2]
[1]International Institute of Information Technology Bangalore, [2]International Institute of Information Technology-Bangalore

2:40PM
2B.4
A PPA- and Security-aware Physical Design Flow
Chun-Wei Chiu and Ting-Chi Wang
National Tsing Hua University

3:00PM
2B.5
The Impact of Logic Locking on Confidentiality: An Automated Evaluation
Lennart Reimann[1], Evgenii Rezunov[1], Dominik Germek[2], Luca Collini[3], Christian Pilato[4], Ramesh Karri[3], Rainer Leupers[1]
[1]RWTH Aachen University, [2]Corporate Research Robert Bosch GmbH, [3]NYU Tandon School of Engineering, [4]Politecnico di Milano

SESSION 2C

Wednesday April 23

Efficient Hardware Architectures for AI and Approximate Computing

Chair: **Ahmedullah Aziz**, The University of Tennessee, Knoxville

1:40PM
2C.1
Efficient Self-Supervised Continual Learning with Progressive Task-correlated Layer Freezing
Li Yang[1], Sen Lin[2], Fan Zhang[3], Junshan Zhang[4], Deliang Fan[5]
[1]university of north carolina at charlotte, [2]University of Houston, [3]Johns Hopkins University, [4]University of California, Davis, [5]Arizona State University

2:00PM
2C.2
Bitwise Systolic Array Architecture for Runtime-Reconfigurable Multi-precision Quantized Multiplication on Hardware Accelerators
Yuhao Liu[1], Salim Ullah[2], Akash Kumar[2]
[1]Technische Universitaet Dresden, [2]Ruhr-Universitaet Bochum

2:20PM
2C.3
LibApprox: A Comprehensive Library for Performance Efficient Approximate Circuits
Bhargav D V[1], Dantu Nandini Devi[2], Rachana Kaparthi[1], Madhav Rao[1]
[1]International Institute of Information Technology-Bangalore, [2]International Institute of Information Technology Bangalore

2:40PM

2C.4

Meta-Heuristic Optimization for Designing Error Diluted Weight Stationary Approximate Systolic Array Architecture

Dantu Nandini Devi[1], Bindu G Gowda[2], Madhav Rao[3]

[1]International Institute of Information Technology Bangalore, [2]International Institute of Information Technology, Bangalore, [3]International Institute of Information Technology-Bangalore

3:00PM

2C.5

Design of Hardware-Efficient Inexact Multiplier Using Evolutionary Algorithm Factored by Multi-variate Approximation

Dantu Nandini Devi[1], Saketh Gajawada[2], Madhav Rao[3]

[1]International Institute of Information Technology Bangalore, [2]InternationalInstituteofInformationTechnologyBangalore, [3]International Institute of Information Technology-Bangalore

SESSION PW1

Thursday April 24

Short Presentation & WIP Session 1

Chair: **Avani Dave**, Intel Corp.

9:40AM

PW1.1

Area-optimized 2D Interleaved Adder Tree Design for Sparse DCIM Edge Processing

Akash Sankhe[1], Mukul Lokhande[1], Radheshyam Sharma[1], Santosh Vishvakarma[2]

[1]Indian Institute of Technology Indore, [2]IIT Indore

9:45AM

PW1.2

Hardware and Algorithm Codesign for Efficient Gaze Tracking in Virtual Reality System

Sai Qian Zhang, Wenxuan Liu, Haiyu Wang

New York University

9:50AM

PW1.3

Reinforcement Learning for Testtime Optimization in the Network-on-Chip based Systems

Anantha Ganesh Karikar Kamath[1], Aditya Kulkarni[2], Himanshu Singh[2], Kanchan Manna[3]
[1]BITS Pilani, Goa Campus, [2]Dept. of CSIS, BITS Pilani, Goa Campus, [3]Dept. of CSIS, BITS Pilani Goa Campus

9:55AM

PW1.4

Efficient and Scalable Place and Route Methodology for Large-Scale Hierarchical Designs: Achieving Faster Turnaround Time and Predictability

Subhadeep Aich[1], Rajanikant Sakariya[2], Vivek Joshi[1]
[1]Texas Instruments, [2]Texas Instruments (India) Pvt. Ltd.

10:00AM

PW1.5

Die Area Reduction by Decongesting Top Channels Using Novel Feedthrough Insertion Methodology in Hierarchical SoC Designs

Rajanikant Sakariya[1], Subhadeep Aich[1], Vivek Joshi[1], Roger Griesmer[2]
[1]Texas Instruments (India) Pvt. Ltd., [2]Texas Instruments Incorporated

10:05AM

PW1.6

DT2HDL: A Binary Decision Tree to HDL Generation tool

Qijia Tang, Dinesh Pamunuwa, Roshan Weerasekera
University of Bristol

10:10AM

PW1.7

Adding Context to LLM-Guided Verilog Repair

Abdelrahman Elnaggar and Benjamin Tan
University of Calgary

10:15AM

PW1.8

A Max Weighted-Matching based Non-Greedy Post-HLS Power Gating Technique with Comprehensive Power Modeling

Xiuyan Zhang and Shantanu Dutt

University of Illinois at Chicago

10:20AM

PW1.9

Therunet-SP: 2.5D IC Thermal Simulation Using U-Net Convolution and Scaling Procedure

Yu-Min Lee, Shun-Ping Huang, Ying-Hui Lin

National Yang Ming Chiao Tung University

10:25AM

PW1.10

MErBAG: Mesh Error Based Adaptive Grid Generation in System-Level Thermal Analysis

Yu-Min Lee, Shih-Chieh Hsu, Bo-Yi Tsai, Zong-Lin Lu

National Yang Ming Chiao Tung University

SESSION PW2

Thursday April 24

Short Presentation & WIP Session 2

Chair: **Hao Jiang**, San Francisco State University

9:40AM
PW2.1
Illuminati: A Simulation Framework for Modeling and Evaluating Photonic Neural Networks
Andy Wolff and Avinash Karanth
Ohio University

9:45AM
PW2.2
Evaluating LLM-based Communicative Agents for Verilog Design
Parker Link and Benjamin Tan
University of Calgary

9:50AM
PW2.3
Weighted Vertex Cover Using Disjoint Set Data Structures for the Memory Reconfiguration Problem
Rouwaida Kanj
Synopsys

9:55AM
PW2.4
Guardians of the Quantum GAN
Archisman Ghosh[1], Debarshi Kundu[2], Avimita Chatterjee[2], Swaroop Ghosh[2]
[1]The Pennsylvania State University, [2]Pennsylvania State University

10:00AM

PW2.5

Graphene-Based FPGA Design and Optimization at the 7nm FinFET Technology Node

Sheng Lu[1], Zhenlin Pei[1], Liuting Shang[2], Sungyong Jung[3], Qilian Liang[2], Chenyun Pan[2]
[1]The University of Texas at Arlington, [2]University of Texas at Arlington, [3]South Dakota State University

10:05AM

PW2.6

Function Approximation Using Analog Building Blocks in Flexible Electronics

Paula Lozano Duarte[1], Aradhana Dube[1], Georgios Zervakis[2], Mehdi Tahoori[1], Sani Nassif[3]
[1]Karlsruhe Institute of Technology, [2]University of Patras, [3]Radyalis

10:10AM

PW2.7

Deep Learning-Based ASM-ESD Forward I-V Parameter Extraction

Fredo Chavez and Sourabh Khandelwal
Macquarie University

10:15AM

PW2.8

Exploring Parallel Implementation of SPHINCS+ using Advanced Vector Extensions (AVX) Sets

Yaoyun Zhou, Kavin Rajasekaran, QIAN WANG
University of California, Merced

10:20AM

PW2.9

Cross-Layer EM Fault Injection Assessment Framework

Hanqiu Wang[1], Ruochen Dai[1], Tuba Yavuz[1], Xiaolong Guo[2], Orlando Arias[3], Dean Sullivan[4], Siqi Dai[1], Honggang Yu[1], Michael Lee[1], Domenic Forte[1], Shuo Wang[1]
[1]University of Florida, [2]Electrical and Computer Engineering Department, Kansas State University, [3]University of Massachusetts Lowell, [4]University of New Hampshire

10:25AM
PW2.10
Adversarial Assertions
Prabhat Mishra
University of Florida

SESSION PW3

Thursday April 24

Short Presentation & WIP Session 3

Chair: **Sushant Sadangi**, Intel Corporation

9:40AM
PW3.1
Optimizing Post-quantum Crypto Algorithms in Embedded IoT Systems with QUIC Protocol
Ben Dong and QIAN WANG
University of California, Merced

9:45AM
PW3.2
Analysis of the Impact of LFSR Architecture on Accuracy of Stochastic Computing Processors
Seongmo An, Sangho Lee, Jinyoung Shin, Yue Ri Jeong, Seung Eun Lee
Seoul National University of Science and Technology

9:50AM
PW3.3
Aging Attack on Systolic Array-based AI accelerators via NBTI-Induced Aging
Masoud Heidary and Biresh Kumar Joardar
University of Houston

9:55AM

PW3.4

Analysis of Short and Aging Faults in TSVs at the Physical Level with Parametric Variation

Prosen Kirtonia[1], Shelby Williams[1], Prasanna Kawatker[1], Kasem Khalil[2], Magdy Bayoumi[3]
[1]University of Louisiana at Lafayette, [2]University of Mississippi, [3]U. of Louisiana

10:00AM

PW3.5

Energy-Aware DNN Task Scheduling with Dynamic Batching and Frequency Adjustment

Vasileios Pentsos[1], Spyros Tragoudas[2], Kiriti Gowda[3], Mike Schmit[3]
[1]Southern Illinois University of Carbondale, [2]Southern Illinois University Carbondale, [3]Advanced Micro Devices, Inc.

10:05AM

PW3.6

LUTAccel: Look-up-Table based Vector Systolic Accelerator on FPGAs

Aashish Tiwary[1], Saketh Gajawada[2], Jay Shah[3], Nanditha Rao[4]
[1]International Institute of Information Technology, Bangalore, [2]InternationalInstituteofInformationTechnologyBangalore, [3]International Institute of Information Technology Bangalore, [4]IBM

10:10AM
PW3.7
RL-Driven Fine-Grained Power Gating for Modern Processors Using Multi-Layer Perceptron Models
Naman Kalra and Jaynarayan Tudu
IIT Tirupati

10:15AM
PW3.8
RECminThrash : Recency and Eviction Count Based Cache Replacement Policy to Minimize Thrashing at the Last Level Caches
Chetan Kumar[1] and Arijit Nath[2]
[1]Indian Institute of Information Technology, Guwahati, [2]IIIT Guwahati

10:20AM
PW3.9
Precision Unwound: Fine-Tuning Loop Unrolling for Energy-efficient FPGA-based PQC using HLS
Srijeet Guha[1] and Andrea Guerrieri[2]
[1]Nvidia, [2]EPFL and HES-SO

10:25AM
PW3.10
Assertion-Based Trojan Localization Using Iterative Path Sensitization
Suriya Srinivasan, Ranga Vemuri, Andrew Jones, Cameron Hingson, Gannon Darrach
University of Cincinnati

SESSION 3A

Thursday April 24

Simulation and Analysis in VLSI Design

Chair: **Srini Krishnamoorthy**, Intel Corporation

10:45AM
3A.1
DAPP: Delay Aware Power Prediction
Sagar Satapathy and Dip Sankar Banerjee
Indian Institute of Technology Jodhpur

11:05AM
3A.2
Thermal Model Extraction at Chip Boundaries for Thermal Simulation of Chip in a System
Kai-Xiang Lin, Yu-Min Lee, Bo-Yi Tsai
National Yang Ming Chiao Tung University

11:25AM
3A.3
Analysis of VF-TLP ESD Measurements Using Machine Learning
Seyed Hossein Hosseini[1], Mehrdad Nourani[1], Theo Smedes[2], Charvaka Duvvury[3]
[1]The University of Texas at Dallas, [2]NXP Semiconductors, [3]iT2 Technologies

11:45AM
3A.4
Machine Learning-Based Pruning Algorithm of Partitioning Techniques for Circuit Simulation
Qian Chen, Xiaofeng Yang, Shengli Lu
Southeast University

SESSION 3B

Thursday April 24

Recent Trends in Cognitive Computing Hardware

Chair: **Hongyu An**, Michigan Technological University

10:45AM
3B.1
Explainable AI-Guided Efficient Approximate DNN Generation for Multi-Pod Systolic Arrays
Ayesha Siddique[1], Khurram Khalil[1], Khaza Anuarul Hoque[2]
[1]University of Missouri-Columbia, [2]University of Missouri

11:05AM
3B.2
PhotoGAN: Generative Adversarial Neural Network Acceleration with Silicon Photonics
Tharini Suresh, Salma Afifi, Sudeep Pasricha
Colorado State University

11:25AM
3B.3
Keep All in Memory with Maxwell: a Near-SRAM Computing Architecture for Edge AI Applications
Gregoire Eggermann[1], Giovanni Ansaloni[1], David Atienza[2]
[1]EPFL, [2]École Polytechnique Fédérale de Lausanne (EPFL)

11:45AM
3B.4
Efficient digital architecture of spiking encoders for neuromorphic accelerators
Ruizhe Li, Muhammad Farhan Azmine, Gauri Sharma, Yang Yi
Virginia Tech

12:05PM

3B.5

Region Masking to Accelerate Video Processing on Neuromorphic Hardware

Sreetama Sarkar[1], Sumit Shrestha[2], Yue Che[1], Leobardo E Campos Macias[2], Gourav Datta[3], Peter Beerel[4]

[1]University of Southern California, [2]Intel Labs, [3]Case Western Reserve University, [4]Univ. of Southern California

SESSION 3C

Thursday April 24

Neuromorphic Computing for Next-gen Machine Intelligence

Chair: **Kang Bai**, AFRL

10:45AM
3C.1
Energy-Efficient Neuromorphic Closed-Loop Modulation System for Parkinson's Disease
Ananna Biswas, Md Akhtaruzzaman, Hongyu An
Michigan Technological University

11:05AM
3C.2
Compressed CNN for Inferring Rapid RF Fingerprints using Memristor Crossbar Array
Josh Li[1], Jianbin Huang[2], Michael Jiang[3], Kang Jun Bai[4]
[1]University of Maryland Baltimore County, [2]San Francisco State University, [3]University of Illinois Urbana-Champaign, [4]Air Force Research Laboratory

11:25AM
3C.3
Modular Approach for Controlling Multi-Agent Systems with Natural Language
Christian Brazeau
Air Force Research Lab Information Directorate (AFRL/RITB)

11:45AM
3C.4
R2CTA: Reinforcement Learning and Reservoir Computing based Chiplets TSV Assignment
Xiaomeng Wang and Cindy Yang Yi
Virginia Tech

SESSION 4A

Thursday April 24

VLSI Physical Design Methodologies

Chair: **Chidhambaranathan Rajamanikkam**, Synopsys Inc.

2:10PM
4A.1
Obstacle-aware Synthesis of the Bus Topology Considering Wire Length Minimization
Meng Lian[1], Yushen Zhang[1], Mengchu Li[1], Tsun-Ming Tseng[1], Shejun Sun[2], Ulf Schlichtmann[1]
[1]Technical University of Munich, [2]Huawei Device Co., Ltd

2:30PM
4A.2
A Comprehensive Approach to Characterizing VT Miscorrelation Derates for Physical Design and Timing Signoff
Pravin Chandran, Hitesh Sharma, Srinivas Bodapati
Intel

2:50PM
4A.3
Open-ALOE: An Analog Layout Automation Flow for the Open-Source Ecosystem
Yueting Li[1], Xingyu Ni[2], Sara Achour[2], Boris Murmann[3]
[1]University of California, Berkeley, [2]Stanford University, [3]University of Hawaii, Mānoa

3:10PM
4A.4
Improving Routability Prediction via NAS Using a Smooth One-shot Augmented Predictor
Arjun Sridhar, Chen-Chia Chang, Junyao Zhang, Yiran Chen
Duke university

SESSION 4B

Thursday April 24

Security Evaluation in Complex Designs

Chair: **Tasnuva Farheen**, Louisiana State University

2:10PM
4B.1
Genetic Algorithm-Assisted Golden-Free Standard Cell Library Extraction from SEM Images
Mengdi Zhu, Ronald Wilson, Reiner Dizon-Paradis, Olivia Dizon-Paradis, Domenic Forte, Damon Woodard
University of Florida

2:30PM
4B.2
A Framework for PCB Design File Reconstruction from X-ray CT Annotations
Carson Sobolewski, David Koblah, Domenic Forte
University of Florida

2:50PM
4B.3
i-Know What You Do: Privacy Evaluation of Apple Smartphones with Remote Acoustic Side-Channels
Oswa Amro, Sanapala Jaswanth, Sai Dishanth Banoth, Urbi Chatterjee
Indian Institute of Technology Kanpur

3:10PM
4B.4
ML-based Real-Time URL Inspection with Hardware Acceleration for Enhanced Web Security
Majid Nezarat[1], Erfan Khedersolh[1], Hadi Shahriar Shahhosseini[1], Amin Rezaei[2]
[1]Iran University of Science and Technology, [2]California State University, Long Beach

3:30PM

4B.5

MATTER: MULTI-STAGE ADAPTIVE THERMAL TROJAN FOR EFFICIENCY & RESILIENCE DEGRADATION

Mehdi Elahi[1], Mohamed R.Elshamy[2], Abdel-Hameed Badawy[2], Mahdi Fazeli[3], Ahamd Patooghy[1]

[1]North Carolina A&T state University, [2]New Mexico state university, [3]Halmstad University

SESSION 4C

Thursday April 24

Generative AI on Edge

Chair: **Amey Kulkarni**, NVIDIA

2:10PM
4C.1
MambaLiteSR: Image Super-Resolution with Low-Rank Mamba using Knowledge Distillation
Romina Aalishah, Mozhgan Navardi, Tinoosh Mohsenin
Johns Hopkins University

2:30PM
4C.2
State of Hardware Fuzzing: Current Methods and the Potential of Machine Learning and Large Language Models
Kevin Immanuel Gubbi[1], Mohammadnavid Tarighat[2], Arvind Sudarshan[2], Inderpreet Kaur[1], Pavan Dheeraj Kota[2], Avesta Sasan[1], Houman Homayoun[2]
[1]University of California, Davis, [2]University of California Davis

2:50PM
4C.3
Dynamic Partial Reconfiguration of FPGAs for Energy-Efficient Machine Learning Inference in IoT Systems
Ethan Chen, Junting Deng, Chia Jen Cheng, Jiachen Xu, John Kan, Yuyi Shen, Vanessa Chen
Carnegie Mellon University

3:10PM
4C.4
Leveraging Generative AI for Platform Hardware Design Automation - Learnings and Recommendations
Srini Krishnamoorthy
Intel Corp.

SESSION 5A

Friday April 25

Memristive and Charge-Trap Devices for Next-Gen Computing

Chair: **Sushant Sadangi**, Intel Corporation

8:40AM
5A.1
Behavioral Model of Charge-Trap Transistors for Neuromorphic Systems
Ataollah Saeed Monir[1], Navid Rezazadeh[2], John Gosson[2], Boris Vaisband[3]
[1]McGill university, [2]Blumind, [3]University of California, Irvine

9:00AM
5A.2
All-Optical Reconfigurable Activation Function based on Saturable Absorption
Oceane Destras[1], Felipe Gohring de Magalhaes[2], Sébastien Le Beux[3], Gabriela Nicolescu[2]
[1]Polytechnique Montreal, [2]Polytechnique Montréal, [3]Concordia University

9:20AM
5A.3
Formal Verification of Error Bounds for Resistive-Switching-based Multilevel Matrix-Vector Multipliers
Kemal Çağlar Coşkun[1], Chandan Kumar Jha[2], Muhammad Hassan[3], Rolf Drechsler[4]
[1]Institute of Computer Science, University of Bremen, [2]University of Bremen, [3]Institute of Computer Science, University of Bremen / DFKI, [4]University of Bremen/DFKI

9:40AM
5A.4
Robust and Efficient NAND-like TST-MRAM with Parallel Write/Read Operations and Reconfigurable PUF Mode
Songhan Zhang, Xianzeng Guo, Yaling Wang, Chao Wang, Bi Wang, Zhaohao Wang
Beihang University

10:00AM
5A.5
A Novel Full Adder Design Using Hybrid Memristor Ratioed Logic
Hussein Fadlallah[1], Rouwaida Kanj[2], Basma Hajri[3]
[1]American University of Beirut, [2]Synopsys, [3]Qualcomm

SESSION 5B

Friday April 25

AI-Driven Embedded Computing and Power-Aware System Design

Chair: **Srini Krishnamoorthy**, Intel Corporation

8:40AM
5B.1
V-SYNC-Aware GPU DVFS Governor for Efficient Game Application Execution on Mobile Devices
En-Ming Huang[1], Yu-Fu Kao[2], Yan-Hong Lu[2], Chun-Yi Lee[3]
[1]Google, Inc./National Taiwan University, [2]Google, Inc., [3]Department of Computer Science and Information Engineering, National Taiwan University

9:00AM
5B.2
Energy-Efficient QoS-Aware Scheduling for S-NUCA Many-Cores
Sudam Wasala[1], Jurre Wolff[1], Yixian Shen[1], Anuj Pathania[1], Clemens Grelck[2], Andy Pimentel[1]
[1]University of Amsterdam, [2]Friedrich Schiller University Jena

9:20AM

5B.3

Deep Neural Network Inference Partitioning in Embedded Hybrid Analog-Digital Systems

Fabian Kreß[1], Julian Hoefer[2], Qiushi Lin[3], Patrick Schmidt[2], Zhenhua Zhu[3], Yu Zhu[3], Tanja Harbaum[4], Yu Wang[3], Juergen Becker[1]

[1]Karlsruhe Institute of Technology - ITIV, [2]Karlsruhe Institute of Technology, [3]Tsinghua University, [4]KIT

9:40AM

5B.4

Real-time Thermal Map Characterization and Analysis for Commercial GPUs with AI Workloads

Jincong Lu[1], Sachin Sachdeva[1], Yuxuan Lin[2], Sheldon Tan[3]

[1]University of California, Riverside, [2]The Overlake School, [3]University of California at Riverside

10:00AM

5B.5

IMU-based Motion Trajectory Reconstruction and Recognition with Dynamic Calibration on Embedded System Platform

Kai-Po Hsu[1], Tsung-Han Lai[1], Yi-Ting Li[1], Wuqian Tang[1], Yun-Ju Lee[2], Yung-Chih Chen[3], Wen-Hsin Chiu[1], Chun-Yao Wang[1]

[1]National Tsing Hua University, [2]National Tsing-Hua University, [3]National Taiwan University of Science and Technology

SESSION 5C

Friday April 25

Design Innovation and Accelaration in the Nanometer Era

Chair: **Rasit Onur Topaloglu**, Adeia

8:40AM
5C.1
Ternary-valued Associative Processor Design
Mira Hout[1], Rouwaida Kanj[2], Ahmed Eltawil[3], Mohammed Fouda[4]
[1]ECE Dept., American University of Beirut,, [2]Synopsys, [3]King Abdullah University of Science and Technology, [4]Rain Neuromorphics Inc.

9:00AM
5C.2
A Time-Borrowing Method for High-Performance Bundled-Data Asynchronous Circuits
Bohan Wang, Zeyang Xu, Lingfeng Zhou, Huiyao Wang, Jinghai Wang, Zhiyi Yu, Shanlin Xiao
Sun Yat-Sen University

9:20AM
5C.3
Machine Learning Assisted Magnetic-core Coupled Inductor Design for Interleaved Buck Converter
Maliha Elma, Navya Goli, Umamaheswara Tida
North Dakota State University

9:40AM
5C.4
A Modified RC and Delay based ESD Clamp Circuit with False-trigger Immunity during normal supply operation.
Naresh Kumar, Divya Agarwal, Rajesh Narwal
STMicroelectronic

SESSION 6A

Friday April 25

Advances in Quantum Computing: Security, Optimization, and AI Integration

Chair: **Srini Krishnamoorthy**, Intel Corporation

10:30AM
6A.1
Watermarking of Quantum Circuits
Rupshali Roy and Swaroop Ghosh
Pennsylvania State University

10:50AM
6A.2
Optimizing Quantum Embedding using Genetic Algorithm for QML Applications
Koustubh Phalak[1], Archisman Ghosh[2], Swaroop Ghosh[1]
[1]Pennsylvania State University, [2]The Pennsylvania State University

11:10AM
6A.3
Quantum Prometheus: Defying Overhead with Recycled Ancillas in Quantum Error Correction
Avimita Chatterjee[1], Archisman Ghosh[2], Swaroop Ghosh[1]
[1]Pennsylvania State University, [2]The Pennsylvania State University

11:30AM
6A.4
AI-driven Reverse Engineering of QML Models
Archisman Ghosh[1] and Swaroop Ghosh[2]
[1]The Pennsylvania State University, [2]Pennsylvania State University

SESSION 6B

Friday April 25

Advanced Signal Processing and AI Acceleration

Chair: **Rasit Onur Topaloglu**, Adeia

10:30AM
6B.1
Accelerating Reliability Analysis for Aging and Self-heating using Machine Learning
Tarek Mohamed[1] and Hussam Amrouch[2]
[1]Semiconductor Test and Reliability (STAR), University of Stuttgart, Stuttgart, Germany., [2]Technical University of Munich (TUM)

10:50AM
6B.2
A Generalized Hardware-Efficient Gabor Wavelet Architecture for Medical Image Processing
Priyanka Agarwal[1], Pruthvi Parate[2], Madhav Rao[3]
[1]IIIT Bangalore, [2]International Institute of Information Technology Bangalore, [3]International Institute of Information Technology-Bangalore

11:10AM
6B.3
Notch filter based Readout Interface for Hall-effect sensors for DC and High-Frequency Currents
Ayesha Hassan, Aireen Amir Jalal, Asma Mahar, Alan Mantooth
University of Arkansas

11:30AM
6B.4
Piecewise-Linear Approximation of Self-Attention and Its Accuracy-Aware Training for Area-Efficient Vision Transformer Inference Accelerator
Teppei Kawamura, Yutaka Masuda, Tohru Ishihara
Nagoya University

SESSION 6C

Friday April 25

Intelligent and Secure Computing for Next-Gen Systems

Chair: **Hossein Sayadi**, California State University, Long Beach

10:30AM
6C.1
Energy-efficient Persistently Secure Block-based Differential Checkpointing for Energy Harvesting Devices
Shyamala Palanisamy[1], Wei Wei[2], Mimi Xie[3]
[1]University of Texas at San Antonio, [2]UTSA, [3]The University of Texas at San Antonio

10:50AM
6C.2
Energy-Adaptive Checkpoint-Free Intermittent Inference for Low Power Energy Harvesting Systems
Sahidul Islam, Wei Wei, Jishnu Banerjee, Chen Pan
The University of Texas at San Antonio

11:10AM
6C.3
Efficient Object Detection from Fused RGB and IR Aerial Images Enhanced by Token Selection
Raghavendra Chitroju Kodanda Saiayyappa, Tanvi Banerjee, Wen Zhang
wright state university

11:30AM
6C.4
Obfuscation-Resistant Hardware Malware Detection: A Stacked Denoising Autoencoder Approach
Zhangying He, Chelsea Fernandes, Hossein Sayadi
California State University, Long Beach

11:50AM
6C.5
Navigating the Trilemma: Security, Power, and Performance Trade-offs in Bluetooth Low Energy
Ning Miao[1], Chongzhou Fang[1], Ruijie Fang[1], Ruoyu Zhang[1], Mahdi Eslamimehr[2], Setareh Rafatirad[3], Hossein Sayadi[4], Houman Homayoun[3]
[1]University of California, Davis, [2]University of California, Los Angeles, [3]University of California Davis, [4]California State University, Long Beach

SESSION 7B

Friday April 25

Optimizing Memory, Power, and Computation for Next-Gen Systems

Chair: **Murthy Palla**, Synopsys Inc.

12:55PM
7B.1
Exploiting The Presence of Abundant Zero Data to Improve NVM Lifespan
Arijit Nath and Harsh Raj
IIIT Guwahati

1:15PM
7B.2
Battery State of Health Estimation Using LLM Framework
Aybars Yunusoglu[1], Dexter Le[2], Karn Tiwari[3], Murat Isik[4], I. Can Dikmen[5], Teoman Karadag[5]
[1]Purdue University, [2]Drexel University, [3]Indian Institute of Science, Bangalore, [4]Stanford University, [5]Temsa Research & Development Center

1:35PM
7B.3
SPEED: Scalable and Predictable EnhancEments for Data Handling in Autonomous Systems
Dongjoo Seo[1], Changhoon Sung[2], Junseok Park[3], Ping-Xiang Chen[1], Bryan Donyanavard[2], Nikil Dutt[1]
[1]University of California, Irvine, [2]San Diego State University, [3]Kookmin University

1:55PM
7B.4
An FPGA-based Emulation Process for Dynamic Quantum Circuits
Yicheng Song and Zeljko Zilic
McGill University

2:15PM
7B.5
Sharp-Edge: A Robust Edge Computing Solution through Performance Monitoring Using Tiny Machine Learning
Mehdi Amininasab[1], Mahdi Fazeli[2], Ahmad Patooghy[3]
[1]Independent Scholar, [2]Halmstad University, [3]North Carolina A&T State University

SESSION 7C

Friday April 25

Hardware Techniques in Quantum Computing Security

Chair: **Yuntao Liu**, Lehigh University

12:55PM
7C.1
Quantum Quandaries: Unraveling Encoding Vulnerabilities in Quantum Neural Networks
Suryansh Upadhyay[1] and Swaroop Ghosh[2]
[1]Penn State University, [2]Pennsylvania State University

1:15PM
7C.2
Stealthy Conditional Trojans in Quantum Circuits
Jayden John, Lakshaman Golla, QIAN WANG
University of California, Merced

1:35PM
7C.3
OPAQUE: Obfuscating Phase in Quantum Circuit Compilation for Efficient IP Protection
Anees Rehman[1], Vincent Langford[2], Jayden John[3], Yuntao Liu[2]
[1]Independent, [2]Lehigh University, [3]UC Merced

1:55PM
7C.4
Exploration of Vulnerabilities of Fault-Tolerant Quantum Computing
Theodoros Trochatos[1], Christopher Kang[2], Frederic Chong[2], Jakub Szefer[3]
[1]Yale University, [2]University of Chicago, [3]Northwestern University

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