Final Program

ISQED

2020
21st International Symposium on

QUALITY ELECTRONIC DESIGN

AI/ML & Electronic Design, Security, Quantum Computing

March 25-26, 2020
Santa Clara Convention Center,
Santa Clara, CA USA

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ISQED'20 is produced and sponsored by the
International Society for Quality Electronic Design

WELCOME TO ISQED'20

On behalf of the *isQED'20* conference and technical committees, we are pleased to welcome you to the 21st anniversary of the International Symposium on Quality Electronic Design.

We are happy to note that after 21 years of successful ISQED events, the industry has slowly started to realize the importance of the concept of quality in electronic design and hyper critical role it plays in creation of secure, reliable, and manufacturable circuits and systems. It's worth to mention that prior to inception of *isQED* in 1998, the lexicon of technical terminologies, hardly contained any combination of "Quality", "Design", and "Electronic" words. Terms such as "Quality Electronic Design", "Quality in Electronic Design", etc. could not be found in any internet search. Then, the concept of "Quality" in design of integrated circuits and systems was a foreign concept that confused even the ardent industry practitioners.

During these 21 years, *isQED* has strived to pioneer a premier interdisciplinary and multidisciplinary design conference, with the goal to bridge the gap among electronic & semiconductor ecosystem disciplines to promote the **Design for Quality (DfQ)**.

isQED'20 is once again being held with the technical sponsorship of the IEEE Electron Devices Society, the IEEE Circuits and Systems Society, and the IEEE Reliability Society. All Conference proceedings & Papers have been published in IEEE Xplore digital library and indexed by Scopus. *isQED* continues to provide and foster a unique opportunity to participants to interact and engage themselves in cutting edge tutorials, presentations, and panel and plenary sessions.

This conference is organized around the key concepts of AI/ML & Electronic Design, Security, IoT, and Quantum Computing. The program consists of five keynote talks, four embedded tutorials and a lunch panel, focusing on these timely and hot topics.

We are pleased to see an increase in the number of papers submitted to the conference this year. The two-day technical program with four parallel sessions packs over 80 peer-reviewed papers highlighting the latest trends in electronic circuit and system design & automation, testing, verification, sensors, security, semiconductor technolo-gies, cyber-physical systems, etc.

All technical presentations, plenary sessions, panel discussions, tutorials and related events will take place on March 25-26 at the Santa Clara Convention Center in Santa Clara, CA USA.
We would like to thank the *isQED'20* corporate sponsors: Synopsys, and Mentor Graphics, for their valuable support of this conference.

Welcome to another exciting *isQED event*! It couldn't have happened without your support and participation.

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ISQED'20 Best Papers

2C.3

Alleviating Bottlenecks for DNN Execution on GPUs via Opportunistic Computing

Xianwei Cheng[1], Hui Zhao[1], Mahmut Kandemir[2], Saraju Mohanty[1] and Beilei Jiang[1]

[1]Department of Computer Science and Engineering, University of North Texas

[2]Department of Computer Science and Engineering, Pennsylvania State University

4C.3

EGAN: A Framework for Exploring the Accuracy vs. Energy Efficiency Trade-off in Hardware Implementation of Error Resilient Applications

Marzieh Vaeztourshizi[1], Mehdi Kamal[2], Massoud Pedram[1]

[1]Ming Hsieh Department of Electrical Engineering, University of Southern California, USA

[2]School of Electrical and Computer Engineering, University of Tehran, Iran

BEST WIP PAPER

PW1.7

A Morphable Physically Unclonable Function and True Random Number Generator using a Commercial Magnetic Memory

Mohammad Nasim Imtiaz Khan, Chak Yuen Cheng, Sung Hao Lin, Abdullah Ash- Saki, and Swaroop Ghosh

School of EECS, Pennsylvania State University, University Park, PA, USA

Authors of best papers are honored during the Synopsys sponsored luncheon on Wednesday March 25.
Ongoing research projects are presented at ISQED under the Work in Progress (WIP) category. This provides a unique opportunity to authors to receive early feedback on their current work.

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Hardware and System Security (HSS)

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Design Technology Co-Optimization (DTCO)

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3 Dimensional Integration & Adv. Packaging (TDIP)

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NOTES

GENERAL INFORMATION

ISQED'20 GENERAL INFORMATION

March 25-26, 2020
Santa Clara Convention Center
5001 Great America Pkwy, Santa Clara, CA 95054

Morning Keynotes

Wednesday, March 25, 9:00 AM - 9:35 AM
Meeting Rooms 203/204

Active Learning for Fast, Comprehensive SPICE Verification

Jeff Dyck
Engineering Director
Mentor, a Siemens Business

Wednesday, March 25, 9:35 AM - 10:10 AM
Meeting Rooms 203/204

Re-Engineering Computing with Neuro-Inspired Learning: Devices, Circuits, and Systems

Prof. Kaushik Roy
Edward G. Tiedemann Jr. Distinguished Professor
Purdue University

Thursday, March 26, 9:00 AM - 9:35 AM
Meeting Rooms 203/204

Spintronic Devices for Memory, Logic, and Neuromorphic Computing

Prof. Joseph S. Friedman
Director of the NeuroSpinCompute Laboratory,
Department of Electrical & Computer Engineering
The University of Texas at Dallas

Thursday, March 26, 9:35 AM - 10:10 AM
Meeting Rooms 203/204

Semiconductors for and by AI

Anwar Awad
Vice President, Infrastructure and Platform Solutions Group, General Manager, Mixed-Signal IP Solution Group
Intel Corporation

Luncheon Keynote

Wednesday, March 25, 12:00 PM - 12:35 PM
Meeting Rooms 203/204

Security as the Enabler of Quality Electronics

Dr. Chi-Foon Chan
President and co-CEO
Synopsys

Luncheon Panel Discussion

Wednesday, March 25, 12:35 PM - 1:50 PM
Meeting Rooms 203/204

Driving forward: Is autonomous vehicle development heading towards a crash?

The automotive industry is going through a disruptive phase and one of the major factors causing this disruption is autonomous cars. The digitalization of the automotive industry is changing the traditional patterns of transport and mobility, and connected vehicles, self-driving vehicles, vehicles that are increasingly connected to the internet and equipped with electromechanical controls are defining some of todays and most of the future automotive industry. Though there is strong demand from users, how realistic is the future of autonomous vehicles? Is the safety of autonomous cars an issue for drivers and will potential safety issues cause the autonomous vehicle development to crash? Is the mobility trend shifting towards ride sharing? What new challenges and opportunities do driverless cars bring to the microelectronic industry? What are the safety and security constraints? What are the implications of the inclusion of AI hardware and software? Join us to listen to our panelist's thoughts on the subject.

Panelists:
Nirmal R. Saxena - NVIDIA
Jan-Philipp Gehrmann - NXP
Burkhard Huhnke - Synopsys
Vaibhav Garg - Texas Instruments
Lee Harrison - Mentor, A Siemens Business

Chairs:
Tuna Tarim - *Texas Instruments (Chair)*
Shigeki Tomishima - *Intel (Co-Chair)*
Mehdi Tahoori - *KIT (Co-Chair)*

Moderator:
Ali Iranmanesh - *Silicon Valley Polytechnic*

GENERAL INFORMATION

ISQED LUNCH & AWARDS CEREMONY

Wednesday, March 25, 11:45 AM - 12:00 PM
Meeting Rooms 203/204

ISQED Best Paper Awards

Recipients of the ISQED'20 Best Paper Awards will be recognized during the luncheon on Wednesday.
The best papers are shown in Page 2 of this document.

Embedded Tutorials

Chair & Moderators:
Shiyan Hu - Michigan Technological University (Chair)
José Pineda de Gyvez - NXP Semiconductors (Co-Chair)
Steven Hsu - Intel Corporation (Co-Chair)

Meeting Rooms 203/204

Tutorial 1

Wednesday, March 25, 2:00PM - 3:00PM

Abundant-Data Computing: The N3XT 1,000X

Prof. Subhasish Mitra, Stanford University

Tutorial 2

Wednesday, March 25, 3:00PM - 4:00PM

Energy-efficient Secure Circuits for Entropy Generation & Cryptography

Dr. Sanu Mathew, Senior Principal Engineer, Intel

Tutorial 3

Thursday, March 26, 1:00PM - 2:00PM

EDA for Quantum Computing

Dr. Leon Stok, IBM Corp., Poughkeepsie, NY

Tutorial 4

Thursday, March 26, 2:00PM - 3:00PM

Bitcoin Demystified: Disrupting Technology or Mafia Haven?

Dr. Eric Peeters, Texas Instruments

TECHNICAL SESSIONS

There are a total of 16 paper sessions held on Wednesday and Thursday. Technical sessions are held in the format of four parallel tracks in **Meeting Rooms 201, 212, 206 & 207**.

Poster & WIP Papers

Poster papers will be on display in the atrium in front of the meeting rooms on Wednesday March 25th from 5:30PM to 7:30PM. In addition authors of poster and WiP papers will give oral presentation of papers in sessions PW1 and PW2 as shown in the program.

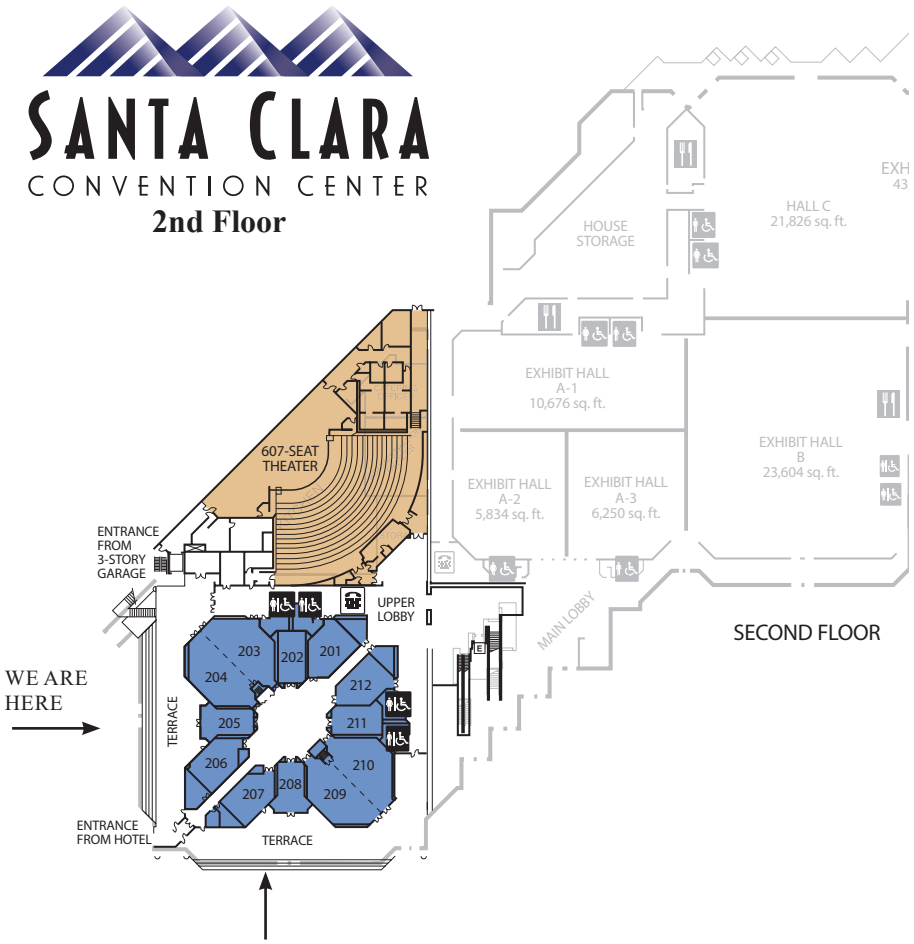
ON-SITE REGISTRATION

Schedule of on-site registration is as follows:

Wednesday, March 25	*8:00 AM - 3:00 PM*
Thursday, March 26	*8:00 AM -1:00 PM*

Registration desk location will be beside the Meeting rooms 203/204.

FLOOR PLAN



Santa Clara Convention Center
2nd Floor
General Sessions, Luncheon & Tutorials:
Meeting Rooms 203/204

Breakout Rooms:
Meeting Rooms, 201, 212, 206 and 207

ISQED'20 PROGRAM AT A GLANCE

DATE	TIME				
WEDNESDAY 3/25/2020	8:45AM -9:00AM	WELCOME AND INTRODUCTION			
		KEYNOTE SPEECH - PLENARY SESSION P1 (MEETING ROOMS 203/204)			
	9:00AM -9:35AM	**ACTIVE LEARNING FOR FAST, COMPREHENSIVE SPICE VERIFICATION** JEFF DYCK - ENGINEERING DIRECTOR, MENTOR, A SIEMENS BUSINESS			
	9:35AM -10:10AM	**RE-ENGINEERING COMPUTING WITH NEURO-INSPIRED LEARNING: DEVICES, CIRCUITS, AND SYSTEMS** PROF. KAUSHIK ROY - EDWARD G. TIEDEMANN JR. DISTINGUISHED PROFESSOR,PURDUE UNIVERSITY			
	10:10AM - 10:25AM	MORNING BREAK			
	10:25AM -11:45AM	SESSION 1A PUF AND SECURITY IN EMERGING SYSTEMS MEETING ROOM 201	SESSION 1B ARTIFICIAL INTELLIGENCE FOR HARDWARE SECURITY MEETING ROOM 212	SESSION 1C RELIABLE ELECTRONICS: FROM EM TO APPROXIMATE COMPUTING MEETING ROOM 206	SESSION 1D MAGNETS AND SPINS FOR BETTER MEMORY MEETING ROOM 207
		ISQED LUNCHEON, KEYNOTE & PANEL MEETING ROOMS 203/204			
	11:45AM -12:00PM	BEST PAPER AWARDS , COMMITTEE RECOGNITION			
	12:00PM -12:35PM	LUNCHEON KEYNOTE **SECURITY AS THE ENABLER OF QUALITY ELECTRONICS** DR. CHI-FOON CHAN, PRESIDENT AND CO-CEO, SYNOPSYS			
	12:35 PM -1:50PM	PANEL DISCUSSION **DRIVING FORWARD: IS AUTONOMOUS VEHICLE DEVELOPMENT HEADING TOWARDS A CRASH?**			
	1:50PM -2:00PM	BREAK			
	2:00PM -3:00PM	EMBEDDED TUTORIAL 1 **ABUNDANT-DATA COMPUTING: THE N3XT 1,000X** MEETING ROOMS 203/204			SESSION WP1 ORAL PRESENTATIONS OF POSTER & WIP PAPERS MEETING ROOM 207
	3:00PM -4:00PM	EMBEDDED TUTORIAL 2 **ENERGY-EFFICIENT SECURE CIRCUITS FOR ENTROPY GENERATION & CRYPTOGRAPHY** MEETING ROOMS 203/204			SESSION WP2 ORAL PRESENTATIONS OF POSTER & WIP PAPERS MEETING ROOM 207
	4:00PM -4:10PM	AFTERNOON BREAK			
	4:10PM -5:30PM	SESSION 2A LOGIC OBFUSCATION AND FAULT ATTACKS MEETING ROOM 201	SESSION 2B RELIABILITY AND PHYSICAL DESIGN MEETING ROOM 212	SESSION 2C NOVEL SYSTEM DESIGN TECHNIQUES MEETING ROOM 206	SESSION 2D ANALOG, NANOTUBE, AND QUANTUM RELEVANCE OF MACHINE LEARNING MEETING ROOM 207
	5:30PM - 6:45PM	POSTER PRESENTATION OF POSTER & WIP PAPERS & MIXER			

ISQED'20 PROGRAM AT A GLANCE

DATE	TIME				
THURSDAY 3/26/20	8:45AM -9:00AM	WELCOME & INTRODUCTION			
		KEYNOTE SPEECH - PLENARY SESSION P2 (MEETING ROOMS 203/204)			
	9:00AM -9:35AM	**SPINTRONIC DEVICES FOR MEMORY, LOGIC, AND NEUROMORPHIC COMPUTING** JOSEPH S. FRIEDMAN - ASSISTANT PROFESSOR, DIRECTOR OF THE NEUROSPINCOMPUTE LABORATORY, DEPARTMENT OF ELECTRICAL & COMPUTER ENGINEERING , THE UNIVERSITY OF TEXAS AT DALLAS			
	9:00AM -9:35AM	**SEMICONDUCTORS FOR AND BY AI** ANWAR AWAD - VICE PRESIDENT, INFRASTRUCTURE AND PLATFORM SOLUTIONS GROUP, GENERAL MANAGER, MIXED-SIGNAL IP SOLUTION GROUP, INTEL CORPORATION			
	10:10AM -10:20AM	MORNING BREAK			
	10:20AM -12:00AM	SESSION 3A SMART SENSORS MEETING ROOM 201	SESSION 3B ARTIFICIAL INTELLIGENCE FOR HARDWARE ACCELERATION MEETING ROOM 212	SESSION 3C.1 CIRCUITS AND SYSTEMS FOR QUANTUM COMPUTING SESSION 3C.2 ARTIFICIAL INTELLIGENCE FOR HARDWARE APPLICATIONS MEETING ROOM 206	SESSION 3D.1 MACHINE LEARNING IN CONVENTIONAL AND EMERGING PLATFORMS SESSION 3D.2 NEUROMORPHIC COMPUTING AND COGNITIVE COMPUTING IN HARDWARE MEETING ROOM 207
	12:00PM - 1:00PM	LUNCH BREAK			
	1:00PM -2:00PM	EMBEDDED TUTORIAL 3 **EDA FOR QUANTUM COMPUTING** MEETING ROOMS 203/204			
	2:00PM -3:00PM	EMBEDDED TUTORIAL 4 **BITCOIN DEMYSTIFIED: DISRUPTING TECHNOLOGY OR MAFIA HAVEN?** MEETING ROOMS 203/204			
	3:00PM - 3:10PM	LUNCH BREAK			
	3:10PM -4:30PM	SESSION 4A.1 3D INTEGRATION & ADVANCED PACKAGING SESSION 4A.2 CIRCUIT AND SYSTEM DIAGNOSIS AND VALIDATION MEETING ROOM 201	SESSION 4B ENERGY ORIENTED SYSTEM DESIGN MEETING ROOM 212	SESSION 4C ENERGY EFFICIENT DESIGNS FOR FUTURE COMPUTING MEETING ROOM 206	SESSION 4D RELIABILITY AND PHYSICAL DESIGN MEETING ROOM 207

ISQED Keynote 1P.1

Wednesday March 25

9:00AM - 9:35AM
Meeting Rooms 203/204

Active Learning for Fast, Comprehensive SPICE Verification Systems

Jeff Dyck
Director of Engineering - Mentor, a Siemens Business

The scope of SPICE-level verification has increased massively with new requirements for safety critical applications, statistical timing characterization, wider FinFET voltage domains, and tighter product margins. We now have many more PVT corners to verify against, and many types of IP need to be verified to high sigma, requiring millions or billions of Monte Carlo samples. Simulation budgets have ballooned and brute-force simulation methods no longer deliver the coverage required within production runtime constraints. For the past 14 years, Solido (now part of Mentor, a Siemens Business) has been using active learning technologies to accelerate SPICE verification by 10X to 1MX, while maintaining SPICE-level accuracy. This talk reviews Solido's active learning techniques used within tools. It provides a deeper dive into the all-new High-Sigma Verifier technology, as well as provides production usage updates from ML Characterization Suite Analytics and Generator.

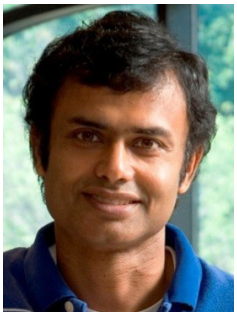
About Jeff Dyck
Jeff Dyck is a Director of Engineering at Mentor, a Siemens Business, responsible for two software product development groups in the integrated circuit verification solutions (ICVS) division. Prior to joining Mentor, Jeff was VP of Engineering at Solido Design Automation, where he led Solido's R&D teams, managed Solido's product lines, and co-invented Solido's machine learning technologies. Solido was acquired by Mentor, a Siemens Business in 2017. Jeff is now working on evolving the active learning technology in Solido's products, as well as developing new disruptively differentiated tools within the Mentor analog mixed signal product line.

Wednesday March 25

9:35AM - 10:10AM

Meeting Rooms 203/204

Re-Engineering Computing with Neuro-Inspired Learning: Devices, Circuits, and Systems



Prof. Kaushik Roy

Edward G. Tiedemann Jr. Distinguished Professor,

Purdue University

Advances in machine learning, notably deep learning, have led to computers matching or surpassing human performance in several cognitive tasks including vision, speech and natural language processing. However, implementation of such neural algorithms in conventional "von-Neumann" architectures are several orders of magnitude more area and power expensive than the biological brain. Hence, we need fundamentally new approaches to sustain exponential growth in performance at high energy-efficiency beyond the end of the CMOS roadmap in the era of 'data deluge' and emergent data-centric applications. Exploring the new paradigm of computing necessitates a multi-disciplinary approach: exploration of new learning algorithms inspired from neuroscientific principles, developing network architectures best suited for such algorithms, new hardware techniques to achieve orders of improvement in energy consumption, and nanoscale devices that can closely mimic the neuronal and synaptic operations of the brain leading to a better match between the hardware substrate and the model of computation. In this presentation, we will discuss our work on spintronic device structures consisting of single-domain/domain-wall motion based devices for mimicking neuronal and synaptic units. Implementation of different neural operations with varying degrees of bio-fidelity (from "non-spiking" to "spiking" networks) and implementation of on-chip learning mechanisms (Spike-Timing Dependent Plasticity) will be discussed. Additionally, we also propose probabilistic neural and synaptic computing platforms that can leverage the underlying stochastic device physics of spin-devices due to thermal noise. System-level simulations indicate ~100x improvement in energy consumption for such spintronic implementations over a corresponding CMOS implementation across different computing workloads. Complementary to the above device efforts, we have explored different learning algorithms including stochastic learning with one-bit synapses that greatly reduces the storage/bandwidth requirement while maintaining competitive accuracy, saliency-based attention techniques that scales the computational effort of deep networks for energy-efficiency and adaptive online learning that efficiently utilizes the limited memory and resource constraints to learn new information without catastrophically forgetting already learnt data.

About Kaushik Roy

Kaushik Roy received B.Tech. degree in electronics and electrical communications engineering from the Indian Institute of Technology, Kharagpur, India, and Ph.D. degree from the electrical and computer engineering department of the University of Illinois at Urbana-Champaign in 1990. He was with the Semiconductor Process and Design Center of Texas Instruments, Dallas, where he worked on FPGA architecture development and low-power circuit design. He joined the electrical and computer engineering faculty at Purdue University, West Lafayette, IN, in 1993, where he is currently Edward G. Tiedemann Jr. Distinguished Professor. He also the director of the center for brain-inspired computing (C-BRIC) funded by SRC/DARPA. His research interests include neuromorphic and emerging computing models, neuro-mimetic devices, spintronics, device-circuit-algorithm co-design for nano-scale Silicon and non-Silicon technologies, and low-power electronics. Dr. Roy has published more than 700 papers in refereed journals and conferences, holds 18 patents, supervised 85 PhD dissertations, and is co-author of two books on Low Power CMOS VLSI Design (John Wiley & McGraw Hill). Dr. Roy received the National Science Foundation Career Development Award in 1995, IBM faculty partnership award, ATT/Lucent Foundation award, 2005 SRC Technical Excellence Award, SRC Inventors Award, Purdue College of Engineering Research Excellence Award, Humboldt Research Award in 2010, 2010 IEEE Circuits and Systems Society Technical Achievement Award (Charles Desoer Award), Distinguished Alumnus Award from Indian Institute of Technology (IIT), Kharagpur, Fulbright-Nehru Distinguished Chair, DoD Vannevar Bush Faculty Fellow (2014-2019), Semiconductor Research Corporation Aristotle award in 2015, and best paper awards at 1997 International Test Conference, IEEE 2000 International Symposium on Quality of IC Design, 2003 IEEE Latin American Test Workshop, 2003 IEEE Nano, 2004 IEEE International Conference on Computer Design, 2006 IEEE/ACM International Symposium on Low Power Electronics & Design, and 2005 IEEE Circuits and system society Outstanding Young Author Award (Chris Kim), 2006 IEEE Transactions on VLSI Systems best paper award, 2012 ACM/IEEE International Symposium on Low Power Electronics and Design best paper award, 2013 IEEE Transactions on VLSI Best paper award. Dr. Roy was a Purdue University Faculty Scholar (1998-2003). He was a Research Visionary Board Member of Motorola Labs (2002) and held the M. Gandhi Distinguished Visiting faculty at Indian Institute of Technology (Bombay) and Global Foundries visiting Chair at National University of Singapore. He has been in the editorial board of IEEE Design and Test, IEEE Transactions on Circuits and Systems, IEEE Transactions on VLSI Systems, and IEEE Transactions on Electron Devices. He was Guest Editor for Special Issue on Low-Power VLSI in the IEEE Design and Test (1994) and IEEE Transactions on VLSI Systems (June 2000), IEE Proceedings -- Computers and Digital Techniques (July 2002), and IEEE Journal on Emerging and Selected Topics in Circuits and Systems (2011). Dr. Roy is a fellow of IEEE.

Luncheon Keynote

Wednesday March 25

12:00PM - 12:35PM
Meeting Rooms 203/204

Security as the Enabler of Quality Electronics

Dr. Chi-Foon Chan
President and co-CEO, Synopsys

Electronics have become ubiquitous in our modern society, running everything from critical infrastructure systems to our cars, phones, and common appliances. Moving new technologies forward will require hardware and software designers and manufacturers to undergo a thorough review to ensure that security is properly accounted for. In his talk, Dr. Chi-Foon Chan will describe how security is influencing the entire industry, and how it is being implemented to enable better quality products.

About Chi-Foon Chan
As Synopsys' co-CEO, Chi-Foon shares responsibility for crafting vision and strategy, leading the company, and ensuring execution excellence in support of our customers' success. As the company's President and COO, a role he held for 14 years prior to his 2012 appointment to President and co-CEO, he guided internal operations and worldwide field organizations. Chi-Foon joined Synopsys in 1990 as Vice President of Applications and Services where he helped build the Technical Field organization. He has sponsored several key initiatives such as entering the IP market, and he personally facilitated key acquisitions such as Avanti, Virage Logic, Magma Design Automation, and SpringSoft. In 2014 he led Synopsys' entry into the software testing market with the acquisition of Coverity, and into the software security market with the acquisition of Codenomicon. Prior to Synopsys, Chi-Foon contributed to industry-leading companies like NEC Corporation, where he was General Manager of the microprocessor group, responsible for marketing all NEC chip devices in North America. Prior to NEC, he was an engineering manager at Intel Corporation. He holds an M.S. and a Ph.D. in Computer Engineering from Case Western Reserve University; and a B.S. in Electrical Engineering from Rutgers University.

Panel Discussion

Wednesday March 25

12:35PM –1:50PM
Meeting Rooms 203/204

Driving forward: Is autonomous vehicle development heading towards a crash?

Panel Committee:
Tuna Tarim - *Texas Instruments (Chair)*
Shigeki Tomishima, *Intel Corporation (Co-Chair)*
Mehdi Tahoori, *KIT (Co-Chair)*

Summary: The automotive industry is going through a disruptive phase and one of the major factors causing this disruption is autonomous cars. The digitalization of the automotive industry is changing the traditional patterns of transport and mobility, and connected vehicles, self-driving vehicles, vehicles that are increasingly connected to the internet and equipped with electromechanical controls are defining some of todays and most of the future automotive industry. Though there is strong demand from users, how realistic is the future of autonomous vehicles? Is the safety of autonomous cars an issue for drivers and will potential safety issues cause the autonomous vehicle development to crash? Is the mobility trend shifting towards ride sharing? What new challenges and opportunities do driverless cars bring to the microelectronic industry? What are the safety and security constraints? What are the implications of the inclusion of AI hardware and software? Join us to listen to our panelist's thoughts on the subject.

Panelists:
Nirmal R. Saxena - NVIDIA
Jan-Philipp Gehrmann - NXP
Burkhard Huhnke - Synopsys
Vaibhav Garg - Texas Instruments
Lee Harrison - Mentor, A Siemens Business

Modedrator:
Ali A. Iranmanesh - Silicon Valley Polytechnic

ISQED Keynote 2P.1

Thursday March 26

9:00AM - 9:35AM
Meeting Rooms 203/204

Spintronic Devices for Memory, Logic, and Neuromorphic Computing

Joseph S. Friedman
Assistant Professor, Director of the NeuroSpinCompute Laboratory,
Department of Electrical & Computer Engineering , The University of Texas at Dallas

Given the impending end of CMOS scaling and its accompanying performance improvements, future advances in computing are contingent on the development of emerging technologies. Spintronics, in which electron spin is manipulated in addition to electron charge, is particularly intriguing due to the availability of non-volatility and the wide range of spintronic switching mechanisms. This presentation will provide an overview of spintronic devices and their application to memory, logic, and neuromorphic computing. The non-volatility inherent to many ferromagnetic structures has been exploited in magnetoresistive random-access memory based on spin-transfer torque, with recent progress towards improved endurance and switching energy through spin-orbit torque switching. Additionally, several approaches have been proposed to use spintronic devices to modulate the switching behavior of other spintronic devices, enabling integrated logic circuits with the potential for energy-efficient high-performance beyond-CMOS computing systems. Finally, non-volatile spintronic devices can be used to emulate the behavior of synapses and neurons in neuromorphic systems modeled on neurobiological structures, providing the opportunity to directly implement neural networks for artificial intelligence and machine learning applications.

About Joseph S. Friedman
Dr. Joseph S. Friedman is an assistant professor of Electrical & Computer Engineering at The University of Texas at Dallas and director of the NeuroSpinCompute Laboratory. He holds a Ph.D. and M.S. in Electrical & Computer Engineering from Northwestern University and undergraduate degrees from Dartmouth College. He was previously a summer faculty fellow at the U.S. Air Force Research Laboratory, a visiting professor at Politenico di Torino, a CNRS research associate with Université Paris-Saclay, a guest scientist at RWTH Aachen University, and worked on logic design automation at Intel Corporation. He is a member of the editorial board of the Microelectronics Journal, the technical program committees of DAC, SPIE Spintronics, NANOARCH, GLSVLSI, and ICECS, and the ISCAS review committee. He has also been a member of the organizing committee of NANOARCH 2019 and DCAS 2018, and was awarded a Fulbright Postdoctoral Fellowship.

Thursday March 26

9:35AM - 10:10AM

Meeting Rooms 203/204

Semiconductors for and by AI

Anwar Awad

Vice President, Infrastructure and Platform Solutions Group, General Manager, Mixed-Signal IP Solution Group, Intel

Artificial Intelligence and Machine Learning are becoming main stream in every aspect of the business and operational world. Markets and companies are using multi-dimensional data to manage their customers and businesses resulting in data explosion. In addition, the role of edge in AI is changing. The future of AI and its adoption needs a re-think and transformation of the hardware industry. The keynote will highlight some of these directions of the hardware industry. In this presentation, Anwar will also highlight the role of Machine Learning in chip design, validation and testing and how we will extend further in the near future to the era of machines designing chips.

About Anwar Awad

Anwar Awad is vice president in the Infrastructure and Platform Solutions Group (IPSG) and general manager of the Mixed-Signal IP Solution Group at Intel Corporation. In this role, Awad is responsible for IP block development and delivery for all mixed-signal IP to all Intel products and segments to ensure the competitiveness of Intel's mixed-signal IP relative to the industry. Awad joined Intel from Synopsys, where he served as vice president of Research and Development, managing the company's mixed-signal IP and digital IP. A 28-year veteran of the tech industry, Awad possess a wide breadth of management and leadership experience in the build of mixed-signal IP development and product lines. He has led multiple engineering teams in areas such as SoC integration, IP CAE, technology porting and integration, and foundry. Awad earned his bachelor's degree in electrical engineering from the University of Jordan and his master's degree in electrical engineering from Stony Brook University in New York.

Embedded Tutorial 1

Wednesday March 25

2:00PM - 3:00PM

Meeting Rooms 203/204

Abundant-Data Computing: The N3XT 1,000X

Prof. Subhasish Mitra

Stanford University

Summary: The world's appetite for analyzing massive amounts of data (streaming video and audio, natural languages, real-time sensor readings, contextual environments or even brain signals) is growing dramatically. The computation demands of these abundant-data applications, such as machine learning, far exceed the capabilities of today's computing systems, and can no longer be met by isolated improvements in transistor technologies, memories or integrated circuit architectures alone. To achieve unprecedented functionality, speed and energy efficiency, one must create transformative NanoSystems which exploit unique properties of underlying nanotechnologies to implement new architectures. We will present the N3XT (Nano-Engineered Computing Systems Technology) approach that enables such NanoSystems through: (i) new computing system architectures leveraging emerging device (logic and memory) nanotechnologies and their dense 3D integration with fine-grained connectivity for computation immersed in memory, (ii) new logic devices (such as carbon nanotube field-effect transistors for implementing high-speed and low-energy logic circuits) as well as high-density non-volatile memory (such as resistive RAM that can store multiple bits inside each memory cell), amenable to (iii) ultra-dense (monolithic) 3D integration of thin layers of logic and memory devices that are fabricated at low temperature. In addition, special techniques overcome imperfections, variations and reliability challenges in such logic, memory and 3D integration technologies. A wide variety of N3XT hardware prototypes (built in research facilities and also in US foundry as part of DARPA's 3DSoC program) represent leading examples of transforming scientifically-interesting nanomaterials and nanodevices into actual NanoSystems. N3XT NanoSystems target 1,000X system-level energy-delay product benefits especially for abundant-data applications. Such massive benefits enable a wide range of applications that push new frontiers, from deeply-embedded computing systems all the way to the cloud.

About Subhasish Mitra

Subhasish Mitra is Professor of Electrical Engineering and of Computer Science at Stanford University. He directs the Stanford Robust Systems Group, co-leads the Computation focus area of the Stanford SystemX Alliance, and is a faculty member of the Wu Tsai Neurosciences Institute. Prof. Mitra also holds the Carnot Chair of Excellence in NanoSystems at CEA-LETI in Grenoble, France. His research ranges across robust computing, NanoSystems, Electronic Design Automation, and neurosciences. Results from his research group have been widely deployed by industry and have inspired significant development efforts by government and research organizations in multiple countries. Jointly with his students and collaborators, Prof. Mitra demonstrated the first carbon nanotube computer and the first three-dimensional NanoSystem with computation immersed in data storage. These demonstrations received wide-spread recognition: cover of NATURE, Research Highlight to the United States Congress by the National Science Foundation, and highlight as "important, scientific breakthrough" by news organizations around the world. In the field of robust computing, Prof. Mitra and his students created key approaches for soft error resilience, circuit failure prediction, on-line self-test and diagnostics, and QED (Quick Error Detection) design verification and system validation. His earlier work on X-Compact test compression at Intel Corporation has proven essential to cost-effective manufacturing and high-quality testing of almost all electronic systems across the industry. X-Compact and its derivatives have been implemented in widely-used commercial Electronic Design Automation tools. Prof. Mitra's honors include the ACM SIGDA / IEEE CEDA Newton Technical Impact Award in Electronic Design Automation (a test of time honor), the Semiconductor Research Corporation's Technical Excellence Award (for innovation that significantly enhances the semiconductor industry), the Intel Achievement Award (Intel's highest corporate honor), and the United States Presidential Early Career Award for Scientists and Engineers from the White House. He and his students have published award-winning papers at major venues: ACM/IEEE Design Automation Conference, IEEE International Solid-State Circuits Conference, ACM/IEEE International Conference on Computer-Aided Design, IEEE International Test Conference, IEEE Transactions on CAD, IEEE VLSI Test Symposium, and the Symposium on VLSI Technology. At Stanford, he has been honored several times by graduating seniors "for being important to them during their time at Stanford." Prof. Mitra has served on the Defense Advanced Research Projects Agency's (DARPA) Information Science and Technology Board as an invited member. He is a Fellow of the Association for Computing Machinery (ACM) and the Institute of Electrical and Electronics Engineers (IEEE).

Embedded Tutorial 2

Wednesday March 25

3:00PM - 4:00PM

Meeting Rooms 203/204

Energy-efficient Secure Circuits for Entropy Generation & Cryptography

Dr. Sanu Mathew

Intel Corporation

Summary: Physically Unclonable Functions (PUF) and True Random Number Generators (TRNG) are foundational security primitives underpinning the root of trust in computing platforms. Contradictory design strategies to harvest static and dynamic entropies typically necessitate independent PUF and TRNG circuits, adding to design cost. This tutorial describes a unified static and dynamic entropy generator leveraging a common entropy source for simultaneous PUF and TRNG operation. We will present self-calibration techniques to run-time segregate bitcells into PUF and TRNG candidates, along with entropy extraction techniques to maximize TRNG entropy while stabilizing PUF bits. Cryptographic circuits such as Advanced Encryption Standard (AES) are vulnerable to correlation power analysis (CPA) side-channel attacks (SCA), where an adversary monitors supply current signatures of a chip to decipher the value of embedded keys. This tutorial will also discuss the use of arithmetic/circuit countermeasures to minimize the correlation of the AES current to embedded keys, thereby improving the SCA resistance of the hardware by 1200x in both time and frequency-domains.

About Sanu Mathew

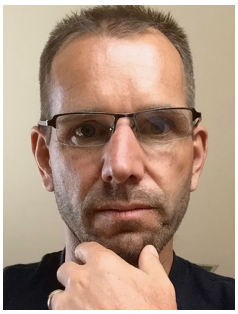
Sanu Mathew is a Senior Principal Engineer with the Circuits Research Labs at Intel Corporation, Hillsboro, Oregon, where he heads the security arithmetic circuits research group, responsible for developing special-purpose hardware accelerators for cryptography and security. He received his Ph.D. degree in Electrical and Computer Engineering from State University of New York at Buffalo in 1999. He holds 62 issued patents, has 20 patents pending and has published over 80 conference/journal papers. He is a Fellow of the IEEE.

Embedded Tutorial 3

Thursday March 26

1:00PM -2:00PM
Meeting Rooms 203/204

EDA for Quantum Computing



Dr. Leon Stok
IBM Corp., Poughkeepsie, NY

Summary: Though early in its development, quantum computing is now available on real hardware via the cloud through IBM Q Experience. This radically new kind of computing holds open the possibility of solving some problems that are now and perhaps always will be intractable for "classical" computers. As with any new technology there are a lot of open questions. What is the road to Quantum Advantage, e.g. the point where quantum computing shows demonstrable and significant advantage over classical computers and algorithms? What is the status of Quantum computers today? How do we define a full system-metric to measure the performance of a Quantum System? We will discuss what we can do in EDA to improve the performance of Quantum Systems and describe the types of EDA problems where quantum computing might be applied.

About Leon Stok
Leon Stok is Vice President of IBM's Electronic Design Automation group. His team delivers world-class design and verification flows and tools being used to design the world's largest supercomputers, IBM systemZ and Power systems. Prior to this he held positions as director of EDA and executive assistant to IBM's Senior Vice President of Technology and Intellectual Property and executive assistant to IBM's Senior Vice President of the Technology group. Leon Stok studied electrical engineering at Eindhoven University of Technology, the Netherlands, from which he graduated with honors in 1986. He obtained a Ph.D. degree from Eindhoven University in 1991. At IBM's Thomas J. Watson Research Center, Leon Stok pioneered logic synthesis, as part of the team that developed BooleDozer. Subsequently, he managed IBM's synthesis group and drove the first commercial application of physical synthesis by developing IBM's Placement Driven Synthesis tool. From 1999-2004 he led all of IBM's design automation research as the Senior Manager Design Automation at IBM Research. He drove key innovations in DFM using RDR (Radically Design Restrictions), in static timing analysis using statistical timing and in large block physical synthesis. Dr. Stok has presented over sixty keynotes, invited talks and tutorials at major IEEE and ACM conferences worldwide and at many leading universities. Dr. Stok has published over sixty papers on many aspects of high level, architectural and logic synthesis, low power design, placement driven synthesis and on the automatic placement and routing for schematic diagrams. He holds 13 patents in EDA. He was elected an IEEE fellow for the development and application of high-level and logic synthesis algorithms.

Thursday March 26

2:00PM - 3:00PM
Meeting Rooms 203/204

Bitcoin Demystified: Disrupting Technology or Mafia Haven?

Dr. Eric Peeters
Texas Instruments

Summary: In this tutorial, we will focus on how bitcoin actually works. Essentially we will cover what is a blockchain. What does "mining coin" mean and how distributed consensus can be achieved. We will cover quickly 2 important concepts in cryptography that enables this technology: hash and signature. We will also discuss attacks that were carried out to stole bitcoins in the past, how and if bitcoin can be used for illegal transactions and finally we will discuss the cost of bitcoins and some alternatives and try to compare it with major centralized existing systems like Visa or Mastercard.

About Eric Peeters
Dr. Eric Peeters received the ME degree in electro-mechanical engineering from University of Louvain-la-Neuve, Belgium, in 2002, and the MSc. and Ph.D. degrees in electrical engineering from the same University in 2004 and 2006, respectively. In 2006, he joined the group Thales Alenia Space ETCA in Belgium for around 1 year. Then, in September 2007, he joined TI Germany in Freising (Munich) to work on the development of security products. In September 2010, he moved to TI headquarters in Dallas where he has been leading the Connected MCU Embedded security group since October 2011 as Security Architect and Manager.

SESSION 1A

Wednesday March 25

PUF and Security in Emerging Systems

Chair: **Nima Karimian**, San Jose State University
Co-Chair: **Jiliang Zhang**, Hunan University

10:25AM
1A.1
Efficient Transfer Learning on Modeling Physical Unclonable Functions
Qian Wang[1], Omid Aramoon[1], Pengfei Qiu[2], Gang Qu[3]
[1]University of Maryland, [2]Research Institute of Information Technology & TNList, Tsinghua University, Beijing, China, [3]Univ. of Maryland, College Park

10:45AM
1A.2
SeqL: Secure Scan-Locking for IP Protection
Seetal Potluri[1], Aydin Aysu[1], Akash Kumar[2]
[1]North Carolina State University, [2]Technical University of Dresden

11:05AM
1A.3
A Survey of DMFBs Security: State-of-the-Art Attack and Defense
Chen Dong[1], Lingqing Liu[1], Huangda Liu[1], Wenzhong Guo[1], Xing Huang[2], Sihuang Lian[1], Ximeng Liu[1], Tsung-Yi Ho[2]
[1]Fuzhou University, [2]National Tsing Hua University

11:25AM
1A.4
How to retrieve PUF response from a fabricated chip securely?
Aijiao Cui and yuxi Wang
Harbin Institute of Technology (Shenzhen)

SESSION 1B

Wednesday March 25

Artificial Intelligence for Hardware Security

Chair: **Hassan Salmani**, Howard University
Co-Chair: **Amey Kulkarni and Abhilash Goyal**, NVIDIA Inc. / Velodyne LiDAR

10:25AM
1B.1
Code-Bridged Classifier (CBC): A Low or Negative Overhead Defense for Making a CNN Classifier Robust Against Adversarial Attacks
Farnaz Behnia[1], ali mirzaeian[1], Mohmmad Sabokrou[2], Sai Manoj[1], Tinoosh Mohsenin[3], Khaled Khasawneh[1], Liang Zhao[1], Houman Homayoun[4], Avesta Sasan[1]
[1]George Mason University, [2]self, [3]University of Maryland Baltimore County, [4]University of California Davis

10:45AM
1B.2
A Survey on Neural Trojans
Yuntao Liu[1], Ankit Mondal[2], Michael Zuzak[1], Abhishek Chakraborty[3], Nina Jacobsen[3], Daniel Xing[3], Ankur Srivastava[3]
[1]University of Maryland, College Park, [2]University of Maryland, [3]University of Maryland College Park

11:05AM
1B.3
LASCA: Learning Assisted Side Channel Delay Analysis for Hardware Trojan Detection
Ashkan Vakil[1], Farnaz Behnia[1], Ali Mirzaeian[1], Houman Homayoun[2], Naghmeh Karimi[3], Avesta Sasan[1]
[1]George Mason University, [2]University of California Davis, [3]University of Maryland Baltimore County

11:25AM
1B.4
Rethinking FPGA Security in the New Era of Artificial Intelligence
Xiaolin Xu
University of Illinois at Chicago

SESSION 1C

Wednesday March 25

Reliable Electronics: From EM to Approximate Computing

Chair: **Raviprakash Rao**, Texas Instruments
Co-Chair: **Marshnil Dave**, Lion Semiconductor

10:25AM
1C.1
CDS-RSRAM: a Reconfigurable SRAM Architecture to Reduce Read Power with Column Data Segmentation
Han Xu[1], Ziru Li[1], Fei Qiao[2], Qi Wei[1], Xinjun Liu[1], Huazhong Yang[1]
[1]Tsinghua University, [2]Dept.of Electronic Engineering in Tsinghua University, Beijing National Research Center for Information Science and Technology (BNRist)

10:45AM
1C.2
RARA: Dataflow Based Error Compensation Methods with Runtime Accuracy-Reconfigurable Adder
Shujuan Yin[1], Zheyu Liu[2], Guihong Li[3], Fei Qiao[2], Qi Wei[4], Yuanfeng Wu[5], Lianru Gao[5], Xinjun Liu[6], Huazhong Yang[2]
[1]Baotou Teachers' College, Inner Mongolia University of Science & Technology, Baotou, China;Tsinghua University, Beijing, China, [2]Tsinghua University, Beijing, China;Beijing National Research Center for Information Science and Technology, [3]University of Texas at Austin;Tsinghua University, Beijing, China, [4]Tsinghua University, Beijing, China, [5]Key Laboratory of Digital Earth Science, Aerospace Information Research Institute, Chinese Academy of Sciences, Beijing, China;, [6]Tsinghua University, Beijing, China;

11:05AM
1C.3
Low-power Accuracy-configurable Carry Look-ahead Adder Based on Voltage Overscaling Technique
Hassan Afzali-Kusha[1], Mehdi Kamal[2], Massoud Pedram[1]
[1]USC, [2]University of Tehran

11:25AM
1C.4
Design Space Exploration Driven by Lifetime Concerns due to Electromigration
Frank Wolff[1], Daniel Weyer[1], Chris Papachristou[1], William Clay[2]
[1]Case Western Reserve University, [2]C.W. Consultants

SESSION 1D

Wednesday March 25

Magnets and Spins for Better Memory

Chair: **Eric Peeters**, Texas Instruments
Co-Chair: **Sara Tehranipoor**, Santa Clara University

10:25AM
1D.1
Integrated CAM-RAM Functionality using Ferroelectric FETs
Sumitha George[1], Nicolas Jao[2], Akshay Krishna Ramanathan[2], Xueqing Li[3], Sumeet Kumar Gupta[4], John Sampson[2], Vijaykrishnan Narayanan[2]
[1]Pennsylvania State University, [2]PSU, [3]Tsinghua University, [4]Purdue University

10:45AM
1D.2
Statistical Analysis of Temperature Variability on the Write Efficiency of Spin-Orbit Torque MRAM using Polynomial Chaos Metamodels
Sonal Shreya[1], Surila Guglani[1], Brajesh Kumar Kaushik[2], Sourajeet Roy[1]
[1]Indian Institute of Technology Roorkee, [2]I.I.T-Roorkee

11:05AM
1D.3
Multi-Bit Read and Write Methodologies for Diode-MTJ Crossbar Array
Mohammad Nasim Imtiaz Khan and Swaroop Ghosh
Pennsylvania State University

SESSION PW1

Wednesday March 25

Posters & WIP Session 1

Chair: **Sara Tehranipoor**, Santa Clara University
Co-Chair: **Vinod Viswanath**, Real Intent, Inc.

2:00PM
PW1.1
Compression or Corruption? A Study on the Effectsof Transient Faults on BNN Inference Accelerators
Navid Khoshavi[1], Connor Broyles[1], Yu Bi[2]
[1]Florida Polytechnic University, [2]University of Rhode Island

2:05PM
PW1.2
A Low-Power LSTM Processor for Multi-Channel Brain EEG Artifact Detection
Hasib-Al- Rashid[1], Nitheesh Kumar Manjunath[1], Hirenkumar Paneliya[1], Morteza Hosseini[1], W. David Hairston[2], Tinoosh Mohsenin[1]
[1]University of Maryland Baltimore County, [2]Human Research and Engineering Directorate, US Army Research Lab

2:10PM
PW1.3
Formal Verification of a Fully Automated Out-of-Plane Cell Injection System
Iram Tariq Bhatti and Osman Hasan
School of Electrical Engineering and Computer Science (SEECS), National University of Sciences and Technology (NUST)

2:15PM
PW1.4
An NBTI-aware Task Parallelism Scheme for Improving Lifespan of Multi-core Systems
Yu-Guang Chen[1], Yu-Yi Lin[2], Ing-Chao Lin[3]
[1]National Central University, [2]Yuan Ze University, [3]National Cheng Kung University

2:20PM
PW1.5
Synthesis and Generalization of Parallel Algorithms Considering Communication Constraints
Akihiro Goda[1], Yukio Miyasaka[2], Amir Masoud Gharehbaghi[3], Masahiro Fujita[2]
[1]1-4-18, [2]University of Tokyo, [3]The University of Tokyo

2:25PM
PW1.6
Optimal choice of waveform for library characterization for accurate delay calculation
Ajoy Mandal and Saili Shete
Texas Instruments

2:30PM
PW1.7
Spintronics-based Reconfigurable Ising Model Architecture
Ankit Mondal and Ankur Srivastava
University of Maryland

2:35PM
PW1.8
A Statistical Methodology for Post-Fabrication Weight Tuning in a Binary Perceptron
Elham Azari[1], Ankit Wagle[1], Sunil Khatri[2], Sarma Vrudhula[1]
[1]Arizona State University, [2]Texas A&M University

2:40PM
PW1.9
Analytical Estimation and Localization of Hardware Trojan Vulnerability in RTL Designs
Sheikh Ariful Islam, Love Kumar Sah, Srinivas Katkoori
University of South Florida

2:45PM
PW1.10
SATConda: SAT to SAT-Hard Clause Translator
Rakibul Hassan, Gaurav Kolhe, Setareh Rafatirad, Houman Homayoun, Sai Manoj Pudukotai Dinakarrao
George Mason University

SESSION PW2

Wednesday March 25

Posters & WIP Session 2

Chair: **Sara Tehranipoor**, Santa Clara University
Co-Chair: **Vinod Viswanath**, Real Intent, Inc.

3:00PM
PW1.1
Entropy-Shield: Side-Channel Entropy Maximization for Timing-based Side-Channel Attacks
Abhijitt Dhavlle[1], Raj Mehta[2], Setareh Rafatirad[2], Houman Homayoun[2], Sai Manoj Pudukotai Dinakarrao[2]
[1]George Mason University , VA, USA, [2]George Mason University

3:05PM
PW1.2
Integrated Implantable Electrode Array and Amplifier Design for Single-chip Wireless Neural Recordings
Hengying Shan[1], Nathan Conrad[1], Shabnam Ghotbi[2], John Peterson[1], Saeed Mohammadi[1]
[1]Purdue University, [2]Purdue Univeristy

3:10PM
PW1.3
IMU-based Smart Knee Pad for Walking Distance and Stride Count Measurement
Teng-Chia Wang[1], Yan-Ping Chang[1], Chun-Jui Chen[1], Yun-Ju Lee[1], Chia-Chun Lin[1], Yung-Chih Chen[2], Chun-Yao Wang[3]
[1]National Tsing Hua University, [2]Yuan Ze University, [3]Dept. CS, National Tsing Hua University

3:15PM
PW1.4
Secure, Scalable and Low-Power Junction Temperature Sensing for Multi-Processor Systems-on-Chip
G ANAND KUMAR
TEXAS INSTRUMENTS INDIA PVT LTD

3:20PM
PW1.5
Saving Time and Energy Using Partial Flash Memory Operations in Low-Power Microcontrollers
Prawar Poudel and Aleksandar Milenkovic
The University of Alabama in Huntsville

3:25PM
PW1.6
Variation-Aware Heterogeneous Voltage Regulation for Multi-Core Systems-on-a-Chip with On-Chip Machine Learning
Joseph Riad[1], Jianhao Chen[1], Edgar Sánchez-Sinencio[1], Peng Li[2]
[1]Texas A&M University, [2]UC Santa Barbara

3:30PM
PW1.7
Performance Boost Scheme with Activated Dummy Fin in 12-nm FinFET Technology for High-Performance Logic Application
Motoi Ichihashi, Jia Zeng, Youngtag Woo, Xuelian Zhu, Chenchen Wang, James Mazza
GLOBALFOUNDRIES

3:35PM
PW1.8
A Morphable Physically Unclonable Function and True Random Number Generator using a Commercial Magnetic Memory
Mohammad Nasim Imtiaz Khan[1], Chak Yuen Cheng[2], Sung Hao Lin[2], Abdullah Ash- Saki[1], Swaroop Ghosh[1]
[1]Pennsylvania State University, [2]The Pennsylvania State University

3:40PM
PW1.9
Extracting Power Signature from Low Dropout Voltage Regulator for IoT Security
David Thompson and Haibo Wang
Southern Illinois University Carbondale

SESSION 2A

Wednesday March 25

Logic Obfuscation and Fault Attacks

Chair: **Samah Saeed**, City University of New York
Co-Chair: **Gang Qu**, University of Maryland

4:10PM
2A.1
Strong Anti-SAT: Secure and Effective Logic Locking
Yuntao Liu[1], Michael Zuzak[1], Yang Xie[1], Abhishek Chakraborty[2], Ankur Srivastava[1]
[1]University of Maryland, College Park, [2]University of Maryland College Park

4:30PM
2A.2
EM Fault Injection on ARM and RISC-V
Mahmoud A. Elmohr, Haohao Liao, Catherine H. Gebotys
University of waterloo

4:50PM
2A.3
On Securing Scan Obfuscation Strategies Against ScanSAT Attack
RAJIT KARMAKAR[1] and Santanu Chattopadhyay[2]
[1]INDIAN INSTITUTE OF TECHNOLOGY KHARAGPUR, [2]IIT Kharagpur

5:10PM
2A.4
Fault Attack Detection in AES by Monitoring Power Side-Channel Statistics
Ahish Shylendra[1], Priyesh Shukla[1], Swarup Bhunia[2], Amit Ranjan Trivedi[1]
[1]University of Illinois at Chicago, [2]University of Florida

SESSION 2B

Wednesday March 25

Reliability and Physical Design

Chair: **Siddartha Nath**, Synopsys Inc.
Co-Chair: **Shipla Pendyala**, Intel Corp.

4:10PM
2B.1
Accurate Estimation of Dynamic Timing Slacks using Event-Driven Simulation
Dimitrios Garyfallou[1], Ioannis Tsiokanos[2], Nestor Evmorfopoulos[1], Georgios Stamoulis[1], Georgios Karakonstantis[2]
[1]University of Thessaly, [2]Queen's University Belfast

4:30PM
2B.2
A Layout-Based Soft Error Rate Estimation and Mitigation in the Presence of Multiple Transient Faults in Combinational Logic
Christos Georgakidis, Georgios Ioannis Paliaroutis, Nikolaos Sketopoulos, Pelopidas Tsoumanis, Christos Sotiriou, Nestor Evmorfopoulos, Georgios Stamoulis
University of Thessaly - Department of Electrical and Computer Engineering

4:50PM
2B.3
Stress-Induced Performance Shifts in Flexible System-in-Foils Using Ultra-Thin Chips
Tengtao Li and Sachin S. Sapatnekar
University of Minnesota

5:10PM
2B.4
A Methodology for Reusable Physical Design
Edward Wang, Colin Schmidt, Adam Izraelevitz, John Wright, Borivoje Nikolic, Elad Alon, Jonathan Bachrach
University of California, Berkeley

SESSION 2C

Wednesday March 25

Novel System Design Techniques

Chair: **Stephen Heinrich-Barna**, Texas Instruments
Co-Chair: **Vinod Viswanath**, Real Intent, Inc.

4:10PM
2C.1
Error Coverage, Reliability and Cost Analysis of Fault Tolerance Techniques for 32-bit Memory in Space Applications
david freitas[1], david mota[1], Daniel Simões[1], Clailton Lopes[1], roger goerl[2], César Marcon[3], Jarbas Silveira[4], João Mota[1]
[1]ufc, [2]PUC-RS, [3]PUCRS, [4]Universidade Federal do Ceará

4:30PM
2C.2
Vulnerability-aware Dynamic Reconfiguration of Partially Protected Caches
Yuanwen Huang and Prabhat Mishra
University of Florida

4:50PM
2C.3
Alleviating Bottlenecks for DNN Execution on GPUs via Opportunistic Computing
Xianwei Cheng[1], Hui Zhao[2], Mahmut Kandemir[3], saraju mohanty[1], Beilei Jiang[2]
[1]University of North Texas, [2]UNT, [3]PSU

5:10PM
2C.4
Learning-Enabled NoC Design for Heterogeneous Manycore Systems
Ryan Kim
Colorado State University

SESSION 2D

Wednesday March 25

Analog, Nanotube, and Quantum Relevance of Machine Learning

Chair: **Sumitha George**, Pennsylvania State University
Co-Chair: **Kurt Schwartz**, Texas Instruments

4:10PM
2D.1
Improving Reliability of Quantum True Random Number Generator using Machine Learning
Abdullah Ash- Saki, Mahabubul Alam, Swaroop Ghosh
Pennsylvania State University

4:30PM
2D.2
Degradation of Classification Accuracy due to Imperfections and Limited Precision and their Mitigation Approaches in Mixed-signal Neuromorphic Image Classifiers
Dmitri Strukov
UC Santa Barbara

4:50PM
2D.3
Reducing Impact of CNFET Process Imperfections on Shape of Activation Function by Using Connection Pruning and Approximate Neuron Circuit
Kaship Sheikh and Lan Wei
University of Waterloo

SESSION PW

Wednesday March 25

Poster & WIP Session

Chair: **Sara Tehranipoor**, Santa Clara University
Co-Chair: **Vinod Viswanath**, Real Intent, Inc.

5:30PM
PW.1
Compression or Corruption? A Study on the Effectsof Transient Faults on BNN Inference Accelerators
Navid Khoshavi[1], Connor Broyles[1], Yu Bi[2]
[1]Florida Polytechnic University, [2]University of Rhode Island

5:30PM
PW.2
A Low-Power LSTM Processor for Multi-Channel Brain EEG Artifact Detection
Hasib-Al- Rashid[1], Nitheesh Kumar Manjunath[1], Hirenkumar Paneliya[1], Morteza Hosseini[1], W. David Hairston[2], Tinoosh Mohsenin[1]
[1]University of Maryland Baltimore County, [2]Human Research and Engineering Directorate, US Army Research Lab

5:30PM
PW.3
Formal Verification of a Fully Automated Out-of-Plane Cell Injection System
Iram Tariq Bhatti and Osman Hasan
School of Electrical Engineering and Computer Science (SEECS), National University of Sciences and Technology (NUST)

5:30PM
PW.4
An NBTI-aware Task Parallelism Scheme for Improving Lifespan of Multi-core Systems
Yu-Guang Chen[1], Yu-Yi Lin[2], Ing-Chao Lin[3]
[1]National Central University, [2]Yuan Ze University, [3]National Cheng Kung University

5:30PM
PW.5
Synthesis and Generalization of Parallel Algorithms Considering Communication Constraints
Akihiro Goda[1], Yukio Miyasaka[2], Amir Masoud Gharehbaghi[3], Masahiro Fujita[2]
[1]1-4-18, [2]University of Tokyo, [3]The University of Tokyo

5:30PM
PW.6
Optimal choice of waveform for library characterization for accurate delay calculation
Ajoy Mandal and Saili Shete
Texas Instruments

5:30PM
PW.7
Spintronics-based Reconfigurable Ising Model Architecture
Ankit Mondal and Ankur Srivastava
University of Maryland

5:30PM
PW.8
A Statistical Methodology for Post-Fabrication Weight Tuning in a Binary Perceptron
Elham Azari[1], Ankit Wagle[1], Sunil Khatri[2], Sarma Vrudhula[1]
[1]Arizona State University, [2]Texas A&M University

5:30PM
PW.9
Analytical Estimation and Localization of Hardware Trojan Vulnerability in RTL Designs
Sheikh Ariful Islam, Love Kumar Sah, Srinivas Katkoori
University of South Florida

5:30PM
PW.10
SATConda: SAT to SAT-Hard Clause Translator
Rakibul Hassan, Gaurav Kolhe, Setareh Rafatirad, Houman Homayoun, Sai Manoj Pudukotai Dinakarrao
George Mason University

5:30PM
PW.11
Entropy-Shield: Side-Channel Entropy Maximization for Timing-based Side-Channel Attacks
Abhijitt Dhavlle[1], Raj Mehta[2], Setareh Rafatirad[2], Houman Homayoun[2], Sai Manoj Pudukotai Dinakarrao[2]
[1]George Mason University , VA, USA, [2]George Mason University

5:30PM
PW.12
Integrated Implantable Electrode Array and Amplifier Design for Single-chip Wireless Neural Recordings
Hengying Shan[1], Nathan Conrad[1], Shabnam Ghotbi[2], John Peterson[1], Saeed Mohammadi[1]
[1]Purdue University, [2]Purdue Univeristy

5:30PM
PW.13
IMU-based Smart Knee Pad for Walking Distance and Stride Count Measurement
Teng-Chia Wang[1], Yan-Ping Chang[1], Chun-Jui Chen[1], Yun-Ju Lee[1], Chia-Chun Lin[1], Yung-Chih Chen[2], Chun-Yao Wang[3]
[1]National Tsing Hua University, [2]Yuan Ze University, [3]Dept. CS, National Tsing Hua University

5:30PM
PW.14
Secure, Scalable and Low-Power Junction Temperature Sensing for Multi-Processor Systems-on-Chip
G ANAND KUMAR
TEXAS INSTRUMENTS INDIA PVT LTD

5:30PM
PW.15
Saving Time and Energy Using Partial Flash Memory Operations in Low-Power Microcontrollers
Prawar Poudel and Aleksandar Milenkovic
The University of Alabama in Huntsville

5:30PM
PW.16
Variation-Aware Heterogeneous Voltage Regulation for Multi-Core Systems-on-a-Chip with On-Chip Machine Learning
Joseph Riad[1], Jianhao Chen[1], Edgar Sánchez-Sinencio[1], Peng Li[2]
[1]Texas A&M University, [2]UC Santa Barbara

5:30PM
PW.17
Performance Boost Scheme with Activated Dummy Fin in 12-nm FinFET Technology for High-Performance Logic Application
Motoi Ichihashi, Jia Zeng, Youngtag Woo, Xuelian Zhu, Chenchen Wang, James Mazza
GLOBALFOUNDRIES

5:30PM
PW.18
A Morphable Physically Unclonable Function and True Random Number Generator using a Commercial Magnetic Memory
Mohammad Nasim Imtiaz Khan[1], Chak Yuen Cheng[2], Sung Hao Lin[2], Abdullah Ash- Saki[1], Swaroop Ghosh[1]
[1]Pennsylvania State University, [2]The Pennsylvania State University

5:30PM
PW.19
Extracting Power Signature from Low Dropout Voltage Regulator for IoT Security
David Thompson and Haibo Wang
Southern Illinois University Carbondale

SESSION 3A

Thursday March 26

Smart Sensors

Chair: **Pradeep Chawda**, Apple, Inc.
Co-Chair: **Abhronil Sengupta**, Pennsylvania State University

10:20AM
3A.1
Rehabilitation System for Limbs using IMUs
Chun-Jui Chen[1], Yi-Ting Lin[1], Chia-Chun Lin[1], Yung-Chih Chen[2], Yun-Ju Lee[1], Chun-Yao Wang[3]
[1]National Tsing Hua University, [2]Yuan Ze University, [3]Dept. CS, National Tsing Hua University

10:40AM
3A.2
Piezoelectric CMOS Charger: Highest Output Power Design
Siyu Yang and Gabriel Rincon-Mora
Georgia Institute of Technology

11:00AM
3A.3
Highest Wireless Power: Inductively Coupled Or RF?
Nan Xing and Gabriel Rincón-Mora
Georgia Institute of Technology

11:20AM
3A.4
Self-Powered IOT System for Edge Inference
Dileep Kurian[1], Tanay Karnik[2], Mukesh Bhartiya[1], saransh Chhabra[2], Saksham Soni[2], Jaykant Timbadiya[2], Suhwan Kim[2], Krishnan Ravichandran[2], Ankit Gupta[2], Angela Nicoara[3]
[1]Intel technologies, [2]Intel, [3]HSLU

11:40AM
3A.5
WiFi for the Internet of Things: Towards Enhancing Energy Efficiency and Timeliness
Behnam Dezfouli
Santa Clara University

SESSION 3B

Thursday March 26

Artificial Intelligence for Hardware Acceleration

Chair: **Amey Kulkarni**, NVIDIA Inc.
Co-Chair: **Abhilash Goyal, Xiaosen Liu**, Velodyne LiDAR / Intel Corp.

10:20AM
3B.1
Optimization using Machine Learning for Heterogeneous Systems
Madhavan Swaminathan
Georgia Tech

10:40AM
3B.2
BNN Pruning: Pruning Binary Neural Network Guided by Weight Flipping Frequency
Yixing Li and Fengbo Ren
Arizona State University

11:00AM
3B.3
CSCMAC - Cyclic Sparsely Connected Neural Network Manycore Accelerator
Hirenkumar Paneliya[1], Morteza Hosseini[1], Avesta Sasan[2], Houman Homayoun[2], Tinoosh Mohsenin[1]
[1]University of Maryland Baltimore County, [2]George Mason University

11:20AM
3B.4
FeFET-Based Neuromorphic Architecture with On-Device Feedback Alignment Training
Sumin Jo[1], Abdullah Zyarah[2], Santoch Kurinec[2], Kai Ni[2], Fatima Tuz Zohora[1], Dhireesha Kudithipudi[1]
[1]University of Texas at San Antonio, [2]Rochester Institute of Technology

11:40AM
3B.5
An Efficient Deep Reinforcement Learning Framework for UAVs
Shanglin Zhou[1], Bingbing Li[1], Caiwu Ding[2], Lu Lu[2], Caiwen Ding[1]
[1]University of Connecticut, [2]New Jersey Institute of Technology

SESSION 3C.1

Thursday March 26

Circuits and Systems for Quantum Computing

Chair: **Pravin Kumar Venkatesan**, Velodyne LiDAR
Co-Chair: **Abhilash Goyal and Amey Kulkarni**, Velodyne LiDAR / NVIDIA Inc.

10:20AM
3C.1.1
Integration and Evaluation of Quantum Accelerators for Data-Driven User Functions
Thomas Hubregtsen[1], Christoph Segler[2], Josef Pichlmeier[3], Aritra Sarkar[4], Thomas Gabor[3], Koen Bertels[4]
[1]BMW Research, [2]BMW Group Research, New Technologies, Innovations, [3]Ludwig Maximilian University of Munich, [4]Delft University of Technology

10:40AM
3C.1.2
Hierarchical Improvement of Quantum Approximate Optimization Algorithm for Object Detection
Junde Li, Mahabubul Alam, Abdullah Ash-Saki, Swaroop Ghosh
Pennsylvania State University

11:00AM
3C.1.3
Cryo-CMOS IC Design and Simulation for Quantum Computing
Jeroen van Dijk[1], Pascal 't Hart[1], Rosario Incandela[1], Bishnu Patra[1], Masoud Babaie[1], Edoardo Charbon[2], Fabio Sebastiano[1], Andrei Vladimirescu[3]
[1]TU Delft, [2]EPFL, Intel Corp, Kavli Institute Delft, [3]University of California at Berkeley/ISEP

SESSION 3C.2

Thursday March 26

Artificial Intelligence for Hardware Applications

Chair: **Pravin Kumar Venkatesan**, Velodyne LiDAR
Co-Chair: **Abhilash Goyal and Amey Kulkarni**, Velodyne LiDAR / NVIDIA Inc.

11:20AM
3C.2.1
Efficient Training of Deep Convolutional Neural Networks by Augmentation in Embedding Space
Mohammad Saeed Abrishami
University of Southern California

11:40AM
3C.2.2
Impacts of Machine Learning on Counterfeit IC Detection and Avoidance Techniques
Omid Aramoon[1] and Gang Qu[2]
[1]University of Maryland, [2]Univ. of Maryland, College Park

SESSION 3D.1

Thursday March 26

Machine Learning in Conventional and Emerging Platforms

Chair: **Sicheng Li**, HPE
Co-Chair: **Navid Khoshavi Najafabadi**, Florida Polytechnic University

10:20AM
3D.1.1
TS-EFA: Resource-efficient High-precision Approximation of Exponential Functions Based on Template-scaling Method
Jeeson Kim, Vladimir Kornijcuk, Doo Seok Jeong
Hanyang University

SESSION 3D.2

Thursday March 26

Neuromorphic Computing and Cognitive Computing in Hardware

Chair: **Sicheng Li**, HPE
Co-Chair: **Navid Khoshavi Najafabadi**, Florida Polytechnic University

10:40AM
3D.2.1
Accurate and Efficient Quantized Reservoir Computing System
Shiya Liu, Yibin Liang, Victor Gan, Lingjia Liu, Yang Yi
Virginia Tech

11:00AM
3D.2.2
A Scalable FPGA Engine for Parallel Acceleration of Singular Value Decomposition
Yu Wang[1], Jeong-Jun Lee[2], Yu Ding[1], Peng Li[3]
[1]Texas A&M University, [2]University of California at Santa Barbara, [3]University of California, Santa Barbara

11:20AM
3D.2.3
Deep Neural Network Based Speech Recognition Systems under Noise Perturbations
Yifang Liu
Smule Inc

SESSION 4A.1

Thursday March 26

3D Integration & Advanced Packaging

Chair: **Ali Shahi**, Global Foundries
Co-Chair: **Sreejit Chakravarty**, Intel Corp.

3:10PM
4A.1.1
Electrostatic Discharge Physical Verification of 2.5D/3D Integrated Circuits
Dina Medhat[1], Mohamed Dessouky[1], DiaaEldin Khalil[2]
[1]Mentor, a Siemens Business / ECE Department, Faculty of Engineering, Ain Shames University, [2]ECE Department, Faculty of Engineering, Ain Shames University

SESSION 4A.2

Thursday March 26

Circuit and System Diagnosis and Validation

Chair: **Sreejit Chakravarty**, Intel Corp.
Co-Chair: **Ali Shahi**, Global Foundries

3:30PM
4A.2.1
Mining Message Flow Specifications using Recurrent Neural Network for System-on-Chip Designs
Yuting Cao[1], Mahesh Ketkar[2], Parijat Mukherjee[2], Hao Zheng[1], Jin Yang[3]
[1]University of South Florida, [2]Intel Corporation, [3]Intel Corportation

3:50PM
4A.2.2
Diagnostic Circuit for Latent Fault Detection in SRAM Row Decoder
Shivendra Singh[1], Varshita Gupta[1], Anuj Grover[1], Kedar Janardan Dhori[2]
[1]Indraprastha Institute of Information Technology Delhi, [2]STMicroelectronics Pvt. Ltd., Greater Noida,

4:10PM
4A.2.3
Signal Selection Heuristics for Post-Silicon Validation
Suprajaa Tummala, Xiaobang Liu, Ranga Vemuri
University of Cincinnati

SESSION 4B

Thursday March 26

Energy Oriented System Design

Chair: **Sourav Das**, Intel Corp.
Co-Chair: **Sara Tehranipoor**, Santa Clara University

3:10PM
4B.1
DOVA: A Dynamic Overwriting Voltage Adjustment for STT-RAM L1 Cache
Jinbo Chen[1], Keren Liu[1], Xiaochen Guo[2], Patrick Girard[3], Yuanqing Cheng[1]
[1]Beihang University, [2]Lehigh University, [3]CNRS, LIRMM

3:30PM
4B.2
Energy-Efficient Edge Detection using Approximate Ramanujan Sums
Archisman Ghosh[1], Gaurav Kumar K[1], Debaprasad De[2], ARNAB RAHA[3], Mrinal Kanti Naskar[1]
[1]Jadavpur University, [2]Techno India, [3]Intel Corporation

3:50PM
4B.3
Comparative Framework for the Analysis of Thermal and Resource Management Algorithms for Multi-Core Architectures
Moeez Akmal[1], Muhammad Sarmad Saeed[1], Muhammad Usama Sardar[2], Hareem Shafi[1], Osman Hasan[1], Heba Khdr[3], Jorg Henkel[3]
[1]National University of Sciences and Technology, Islamabad, Pakistan, [2]Technische Universität Dresden, [3]Karlsruhe Institute of Technology, Karlsruhe, Germany

4:10PM
4B.4
Energy-aware Scheduling of Jobs in Heterogeneous Cluster Systems Using Deep Reinforcement Learning
Amirhossein Esmaili[1] and Massoud Pedram[2]
[1]University of Southern California, [2]USC

SESSION 4C

Thursday March 26

Energy Efficient Designs for Future Computing

Chair: **Swaroop Ghosh**, Pennsylvania State University
Co-Chair: **Vinod Viswanath**, Real Intent, Inc.

3:10PM
4C.1
Two-Graph Approach to Temperature Dependent Skew Scheduling
Mineo Kaneko
Japan Advanced Institute of Science and Technology

3:30PM
4C.2
Spintronics Enabled Neuromorphic Computing: Hardware-Algorithm Co-Design
Kezhou Yang[1], Sen Lu[1], Abhronil Sengupta[2]
[1]Penn State University, [2]The Pennsylvania State University

3:50PM
4C.3
EGAN: A Framework for Exploring the Accuracy vs. Energy Efficiency Trade-off in Hardware Implementation of Error Resilient Applications
Marzieh Vaeztourshizi[1], Mehdi Kamal[2], Massoud Pedram[1]
[1]USC, [2]University of Tehran

4:10PM
4C.4
Insulator-Metal Transition Material Based Artificial Neurons: A Design Perspective
Ahmedullah Aziz[1] and Kaushik Roy[2]
[1]University of Tennessee, Knoxville, [2]Purdue University

SESSION 4D

Thursday March 26

Reliability and Physical Design

Chair: **Shipla Pendyala**, Intel Corp.
Co-Chair: **Siddartha Nath**, Synopsys Inc.

3:10PM
4D.1
NN-PARS: A Parallelized Neural Network Based Circuit Simulation Framework
Mohammad Saeed Abrishami[1], Hao Ge[1], Justin Calderon[1], Massoud Pedram[2], Shahin Nazarian[1]
[1]University of Southern California, [2]USC

3:30PM
4D.2
Layout Capacitance Extraction Using Automatic Pre-Characterization and Machine Learning
Zhixing Li and Weiping Shi
Texas A&M University

3:50PM
4D.3
Asynchronous Design flow for Neuromorphic Chips
Prasad Joshi
Intel Corporation

4:10PM
4D.4
Heterogeneous Integration Platform for AI Applications
Madhavan Swaminathan
Georgia Institute of Technology

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- ***Hardware Security***
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