**ISQED 2013 Tutorial: "Best Design Practices For Modern Integrated Circuits"**

While traditional scaling will take us a few more nodes, drastic changes in the way we design integrated circuits may be needed. For example, 3D interconnects may be needed to decrease communication costs, along with a more aggressive on-chip optical integration.

The tutorial will start by illustrating how AMD designers tackle current advanced nodes. It will then follow with a talk where Oracle researchers show how to integrate optics on chip. Next, Georgia Tech researchers present on design tools and models to design and measure 3D chips.

Novel integrated circuit design furthermore may bring changes in computing architecture. Novel memory techniques may be used as illustrated by a talk from University of Rochester. The tutorial will continue by a talk from NYU-Abu Dhabi on the trending topic of hardware security and how to secure designs and design flows. Furthermore, power management will continue to become essential and work by RealIntent and Intel will be presented to conclude the tutorial.

**9:00-10:40** IC Technology at New Nodes Made Easy
Dr. Alvin Loke (AMD)

**10:50-12:00** Physical Design Considerations for Silicon Nanophotonic Circuits
Dr. Ron Ho (Oracle)

**12:00-1:00** Lunch

**1:00-2:10** Design of 3D ICs: From Concept to Practice
Prof. Sung Kyu Lim (Georgia Tech )

**2:10-3:20** Computer Architecture Design Utilizing Novel Memories
Prof. Engin Ipek (University of Rochester )

**3:40-4:50** Hardware Security and Implications on Design Flows
Prof. Ozgur Sinanoglu (NYU Abu Dhabi)

**4:50-6:00** Holistic Power Management: The Future of Handhelds and other Low Power Devices
Dr. Vinod Viswanath (Realintent), Rajeev D. Muralidhar (Intel, India), and Hari Seshadri (Intel, India)

**Tutorial Chair:** Rasit O. Topaloglu, Ph.D (IBM)

**Title:** IC Technology at New Nodes Made Easy

**Speaker:** Alvin Loke, Ph.D. (AMD)

**Abstract:** Despite increasing economic and technical challenges in scaling CMOS, we continue to witness unprecedented performance with 22-nm fully-depleted tri-gate devices now in production. This tutorial offers a summary of how CMOS device technology has progressed over the past two decades. We will review MOS devices and short-channel fundamentals to motivate how device architectures in production have evolved to incorporate elements such as halos and spaces, mechanical strain engineering, high-K dielectric and metal gate, fully-depleted architectures, and finally tri-gate fins.

**Biography:** Alvin Loke received the BASc (Eng. Physics) degree from the University of British Columbia in 1992, and the MSEE and PhDEE degrees from Stanford University in 1994 and 1999 respectively. From 1998 to 2001, he worked on CMOS technology integration at HP Labs and then at Chartered Semiconductor Manufacturing as an Agilent assignee. In 2001, he transferred to Colorado where he designed CMOS PLL circuits for embedded SerDes and ASIC core clocking. In 2006, he joined Advanced Micro Devices where he has designed wireline circuits and currently addresses analog/mixed-signal concerns for future CMOS. Alvin has authored 40 publications and holds 12 US patents. He served on the 2006-2012 CICC technical program committee and as Guest Editor of the IEEE Journal of Solid-State Circuits. He is presently on the IEEE Solid-State Circuits Society Chapters Committee and an IEEE Distinguished Lecturer.

**Title:** Physical Design Considerations for Silicon Nanophotonic Circuits

**Speaker:** Ron Ho, Ph.D. (Oracle Labs)

**Abstract:** Silicon nanophotonic links have recently captured the attention of designers interested in their potential energy, area, and performance advantages over electrical links. An abstracted view of a silicon nanophotonic link is straightforward, and lends itself nicely to simple and useful system models. Unsurprisingly, however, the realities of building operating photonic links contains several subtleties that are worth understanding. In this talk we will introduce photonic links, discuss their basic operation, and describe the principal physical challenges in their use. These will include resonant ring modulator tradeoffs, ring thermal stability control, efficient receiver designs, and receiver BER vs SNR.

**Biography:** Ron Ho is an Architect at Oracle Labs, working on topics such as off-chip and on-chip communication circuits, memory packaging and architectures, and database acceleration hardware. Previously, he was a Distinguished Engineer and Director at Sun Microsystems, where he was awarded the Sun Microsystems Chairman's Award for Innovation. From 1993 to 2003 he was with Intel Corporation, Santa Clara, CA, where he worked on CPUs ranging from the 80486 to the 3rd generation Itanium processors. He has been on the technical program committees for the IEEE International Solid-State Circuits Conference, Asian Solid-State Circuits Conference, Hot Interconnects Symposium, Asynchronous Circuits and Systems Symposium, and VLSI-Design Automation and Test Conference, and has served as guest editor for both the IEEE Journal of Solid-State Circuits and the IEEE Journal of Selected Topics in Quantum Electronics. He has co-authored over 85 technical conference and journal papers, and has over 45 U.S. patents. He is a member of Tau Beta Pi and Phi Beta Kappa, and was the 1993 IEEE Fortescue Scholar. Ron received his Ph.D. degree in electrical engineering from Stanford University, Stanford, CA.

**Title:** Design of 3D ICs: From Concept to Practice

**Speaker:** Sung Kyu Lim, Ph.D (School of Electrical and Computer Engineering, Georgia Institute of Technology)

**Abstract:** This tutorial covers the design of through-silicon-via (TSV) based three-dimensional integrated circuits. It includes details of numerous “manufacturing-ready” GDSII-level layouts of TSV-based 3D ICs, developed with CAD tools covered in this tutorial. Participants will also learn the sign-off level analysis methodologies for timing, power, signal integrity, and thermo-mechanical reliability for 3D IC designs. Coverage also includes various design-for-manufacturability (DFM), design-for-reliability (DFR), and design-for-testability (DFT) techniques that are considered critical to the 3D IC design process.

**Biography:** Sung Kyu Lim received the B.S., M.S., and Ph.D. degrees from the Computer Science Department, University of California, Los Angeles (UCLA), in 1994, 1997, and 2000, respectively. He joined the School of Electrical and Computer Engineering, Georgia Institute of Technology in 2001, where he is currently an Associate Professor. His research focus is on the architecture, circuit design, and physical design automation for 3D ICs. Dr. Lim received the National Science Foundation Faculty Early Career Development (CAREER) Award in 2006. His work is nominated for the Best Paper Award at ISPD'06, ICCAD'09, CICC’10, DAC'11, DAC’12, and ISLPED’12.

**Title:** Computer Architecture Design Utilizing Novel Memories

**Speaker:** Engin Ipek, Ph.D. (ECE Department, University of Rochester)

**Abstract:** Continued advances in the performance of computer systems depend critically on the industry's ability to scale memory density and capacity for decades to come. Unfortunately, scaling of semiconductor memories is increasingly affected by fundamental limits in deep-submicron process technologies. The ITRS projection predicts difficulties in scaling key DRAM process parameters, and the SIA Roadmap projects difficulties scaling Flash past the 20nm node; at 21 nanometers, small numbers of electrons (e.g., 10) tunneling from the floating gate will cause a Flash cell to lose its state. Recent work differentiates charge memories (such as DRAM, SRAM, and Flash memory), which use electric carriers to store the state of a bit, from resistive memories, which use atomic arrangements to set the resistance of a memory cell to store information. Resistive memories, which include phase-change Memory (PCM), Ferroelectric RAM (FeRAM), Spin-Torque Transfer Magnetoresistive RAM (STT-MRAM), and Resistive RAM (RRAM), the latter of which includes memristors, are all candidates to succeed charge memories if and when charge memories reach fundamental limits. To start exploiting the scalability of resistive memories, however, resistive memories must first be architected to address relatively long latencies, high-energy writes, and finite endurance.

In the first half of this talk, I will examine resistive computation, an architectural technique that aims at developing a new class of power-efficient, scalable systems by migrating much of the functionality of a modern microprocessor from CMOS to STT-MRAM. The key idea is to implement most of the on-chip storage and combinational logic using scalable, leakage-resistant RAM arrays and lookup tables (LUTs) constructed from STT-MRAM to lower leakage, thereby allowing many more active cores under a fixed power budget than a pure CMOS implementation could afford. I will then introduce recent work on architecting PCM as a scalable, persistent DRAM replacement. Software cognizant of this newly provided persistence can provide qualitatively new capabilities. For example, system boot/hibernate will be perceived as instantaneous; application checkpointing will be inexpensive; file systems will provide stronger safety guarantees. Hence, this work is a first step toward a fundamentally new memory hierarchy with deep implications across the hardware-software interface.

**Biography**: Engin Ipek is Assistant Professor of Electrical & Computer Engineering and Computer Science at the University of Rochester, where he leads the Computer Systems Architecture Laboratory. His current research interests are in energy-efficient architectures, high-performance memory systems, and the application of emerging memory technologies to computer systems. Dr. Ipek received his BS (2003), MS (2007), and Ph.D. (2008) degrees
from Cornell University, all in Electrical and Computer Engineering. Prior to joining University of Rochester, he was a researcher in the computer architecture group at Microsoft Research (2007-2009). His work has been recognized by an IEEE Micro Top Picks award, a Communications of the ACM research highlight, an ASPLOS 2010 best paper award, and an NSF CAREER award.

**Title:** Hardware Security and Implications on Design Flows

**Speaker:** Ozgur Sinanoglu, Ph.D. (NYU – Abu Dhabi)

**Abstract:** Today's System on Chip (SoC) is being incorporated with digital, analog, radio frequency, photonic and other devices. More recently, sensors, actuators, and biochips are also being integrated into these already powerful SoCs. On one hand, SoC integration has been enabled by advances in mixed system integration and the increase in the wafer sizes (currently about 300 mm and projected to be 450mm by 2018). Consequently, the cost per chip of such SOCs has reduced. On the other hand, support for multiple capabilities and mixed technologies has increased the cost of ownership of advanced foundries. For instance, the cost of owning a foundry will be $5 billion in 2015. Consequently, only large commercial foundries now manufacture such high performance, mixed system SoCs especially at the advanced technology nodes.

Absent the economies of scale, many of the design companies cannot afford owning and acquiring expensive foundries and hence, outsource their design fabrication to these "one-stop-shop" foundries. This globalization of Integrated Circuit (IC) design flow has introduced security vulnerabilities. If a design is fabricated in a foundry that is outside the direct control of the (fabless) design house, reverse engineering, malicious circuit modification, and Intellectual Property (IP) piracy are possible. An attacker, anywhere in this design flow, can reverse engineer the functionality of an IC/IP, and steal and claim ownership of the IP. An untrusted IC foundry may overbuild ICs and sell the excess parts in the gray market. Rogue elements in the foundry may insert malicious circuits (hardware Trojans) into the design without the designer's knowledge. Because of these and similar hardware-based attacks, the semiconductor industry loses $4 billion annually.

In this talk, we cover Design-for-Trust techniques to regain trust in manufactured hardware. A popular approach to thwart these attacks is to conceal (encrypt) the functionality of an IC while it passes through the different, potentially untrustworthy phases of the global design flow, giving the control back to the designer. We will survey the different approaches to encrypting the functionality of a design. We will then discuss how IC (testing) fault analysis techniques can be used both as a defense aid and as an attack tool. On one hand, we will show how a designer can use VLSI fault analysis to aid the design encryption process. On the other hand, we will show that the fault analysis can be used as a weapon by an attacker to obtain the design functionality. We will also cover side channel measurement based Trojan detection approaches.

**Biography:** Prof. Ozgur Sinanoglu is with the Faculty of Engineering at New York University in Abu Dhabi. Prof. Sinanoglu obtained his Ph.D. in Computer Science and

Engineering from University of California, San Diego, in 2004. During his PhD, he was given the IBM PhD Fellowship Award in two consecutive years in 2001 and 2002, and his PhD thesis won the CSE PhD Dissertation Award in UCSD in 2005. He worked for two years at Qualcomm in San Diego as a senior Design-for-Testability engineer, primarily responsible for developing cost-effective test solutions for low-power SOCs. After a 4-year academic experience at Kuwait University, where he was given two research awards, he has joined in Fall 2010 New York University in Abu Dhabi. Upon spending his integration year as a visiting Faculty in New York at the ECE Department of NYU Poly, he joined the Faculty in AbuDhabi in Fall 2011. His primary field of research is the reliability and security of integrated circuits, mostly focusing on CAD tool development. He has around 100 conference and journal papers in addition to 3 issued and around 10 pending patents. He is also the recipient of the best paper award of VLSI Test Symposium 2011.

**Title:** Holistic Power Management: The Future of Handhelds and other Low Power Devices

**Speakers:** Vinod Viswanath, Rajeev Muralidhar, and Harinarayanan Seshadri

**Abstract:** Power efficiency is a growing concern to all aspects of computing systems ranging from the very small, highly integrated System-on-a-Chip (SoC) based handheld devices to larger systems including servers and many-core high performance computing systems. In order to maximize power optimization, the future trend is to perform holistic power management across different levels of design abstractions. This means that embedded/SoC systems that are power optimized will now be application and workload aware. The O/S will be aware of micro-architectural features to program the device in certain power and sleep states. In this tutorial, we will address the challenges of holistic power management. In particular we'll cover the challenges of a unified specification of power intent across all design abstraction levels; power optimization and holistic power management techniques; and, the challenges of verification of such a system. All three presenters have many years of experience with Intel's low power design methodologies, challenges and state-of-the-art technology. The tutorial will be amply supplemented with real life examples from Intel's experience in designing some of its latest handheld devices.

**Biographies:**

Vinod Viswanath is a Sr. Member of Technical Staff at Real Intent, where he works on the next generation tools to understand and implement low power and timing constraints. Prior to this, he was a researcher in Intel's low power group working on formal verification of processors and SOC platforms. Vinod received his M.S and M.Phil degrees from Yale University and the Ph.D. degree from University of Texas at Austin. His current interests include low power design, specification, and verification at all levels of abstraction and hierarchy. During his 7 years at Intel, Vinod worked on three generations of Intel's Atom line of low power processors, and three generations of low power SoCs intended for handheld devices.

Rajeev Muralidhar is a Platform Software Architect in Intel's Mobile Communications Group, where he has been working on power management architectures for Intel's tablet and smartphone SOC platforms for the last six years. During his last six years at Intel, he has been working on over five generations of SOCs for Intel smartphones/tablets, from design, pre-silicon power modeling/estimation to post-silicon

OS power and performance optimizations. He has several patents in the area of power management/optimizations and has authored/co-authored several papers in the area of power management and cross-layer power optimizations. Previously, he worked in Intel Labs on network processor stacks, stability of internet routing and control plane protocols and quality of service for wired and wireless networks. Rajeev has been with Intel since 2000; he has a Bachelors from NIT, Surathkal (India) and Masters from Rutgers University, both in Computer Engineering. He is also a visiting researcher at Rutgers University's NSF Center for Autonomic Computing, where he collaborates with researchers on power management in large many core systems.

Harinarayanan Seshadri is a Platform Architect in Intel's Mobile Communications Group where he works on software architecture for Smartphones, primarily focusing on power and performance management, platform thermals and energy management. In his current role, he has worked on over five generations of SOCs for Intel's Android and Windows-based smartphones/tablets, in different areas of design, pre-silicon power modeling/estimation, post-silicon OS power and performance optimizations. He has several patents in the area of power management/optimizations. Prior to this, he worked in Digital Enterprise Group, Server Architecture lab and Super computer lab, where he worked on various interconnects technologies, including PCI Express, Infiniband, Intelligent IO and other Enterprise Server technologies like Hot Plug memory, CPU & IO Partitioning etc. He has several papers and patents in these areas. He has been with Intel since 1994.