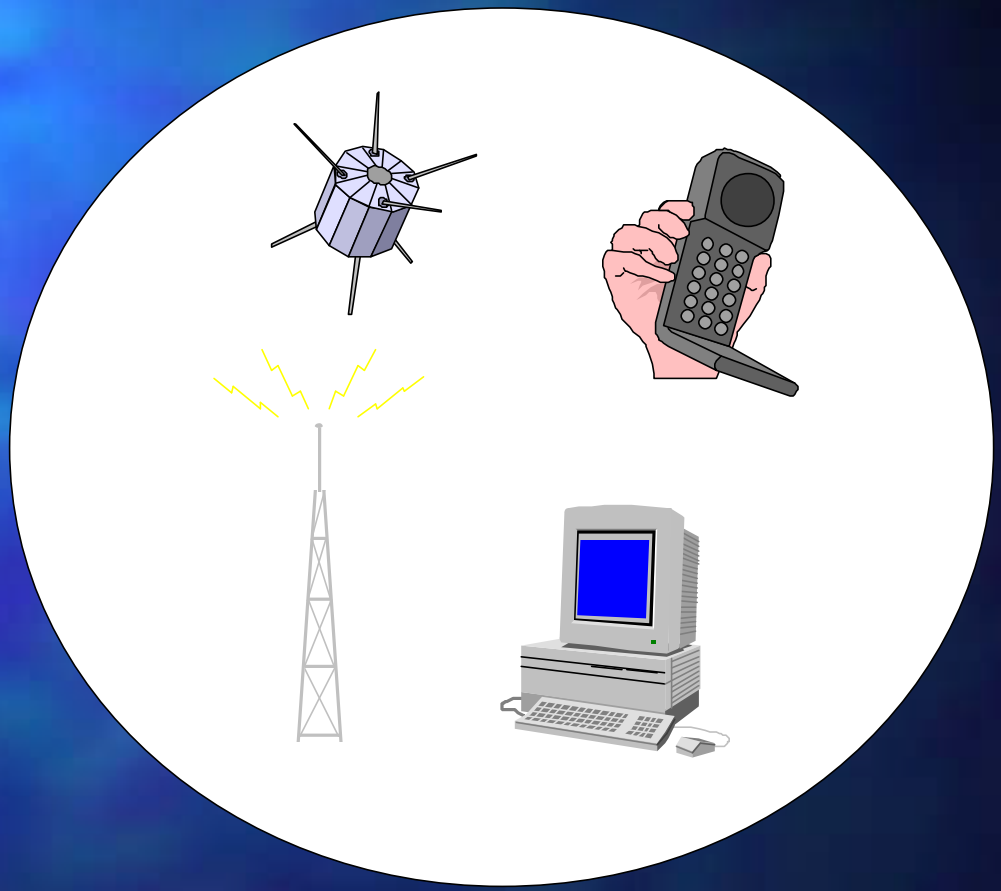
Embedded Quality for Test

Yervant Zorian
LogicVision, Inc.

Electronics Industry

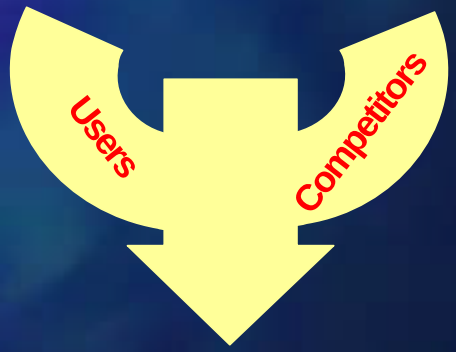
- Achieved Successful Penetration in Diverse Domains



Electronics Industry (cont)

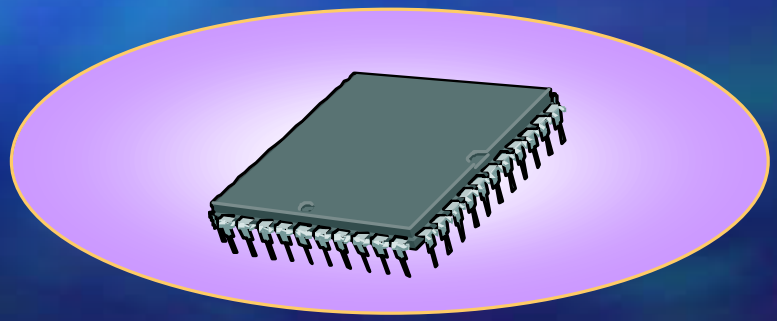
- Met User Quality Requirements
  - satisfying users' to buy products *again*

Created an Unprecedented Dependency
- market-driven product



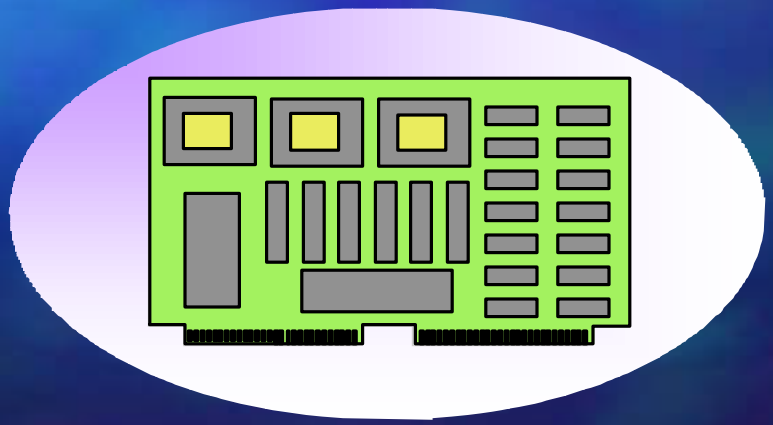
Quality Requirements at Chip Level

- Manufacturing Test for Chips
  - To achieve board defect levels < 1%
  - To maintain ATE cost
- Diagnostics for Chip Manufacturing
  - To enable physical failure analysis
  - To enhance yield by enabling repair for large memories



Quality Requirements at Board Level

- Board Level Manufacturing Test
  - Full Coverage of board level defects
  - Chip failures (handling, stress, infant mortality)
- Diagnostics for Board Level Manufacturing
  - To determine failed interconnect or chip
  - To enable speedy repair



Conventional Test Flow

- Functional Patterns
- Deterministic ATPG with Scan Path
- Full Pin Count Automatic Test Equipment

Emerging Electronics Industry

- Products Shift to Communications and Connectivity

- Maintain competitive edge by providing:
  - Greater Product Functionality
  - Lower Cost (product life cycle)
  - Reduced Time-to-Profitability
  - Higher Quality and Reliability

Emerging Infrastructure

"The internet runs on silicon."

Andy Grove

"The information superhighway is paved in silicon."

Scott McNealey

Emerging Industry Trends

- Caused new technologies:
  - Greater Complexity
  - Increased Performance
  - Higher Density
  - Lower Power Dissipation

The Key Challenge

- To meet Users' Quality Requirements for new Technologies

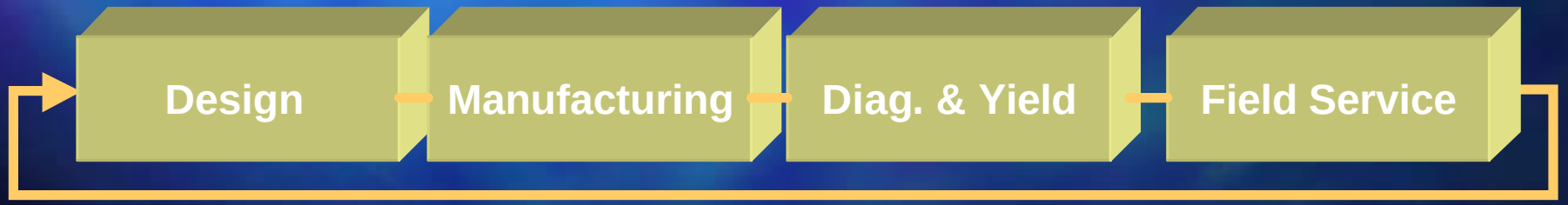
- To assure New Products are adequately:

  Tested, Verified, Measured, Debugged,

  Repaired, ...

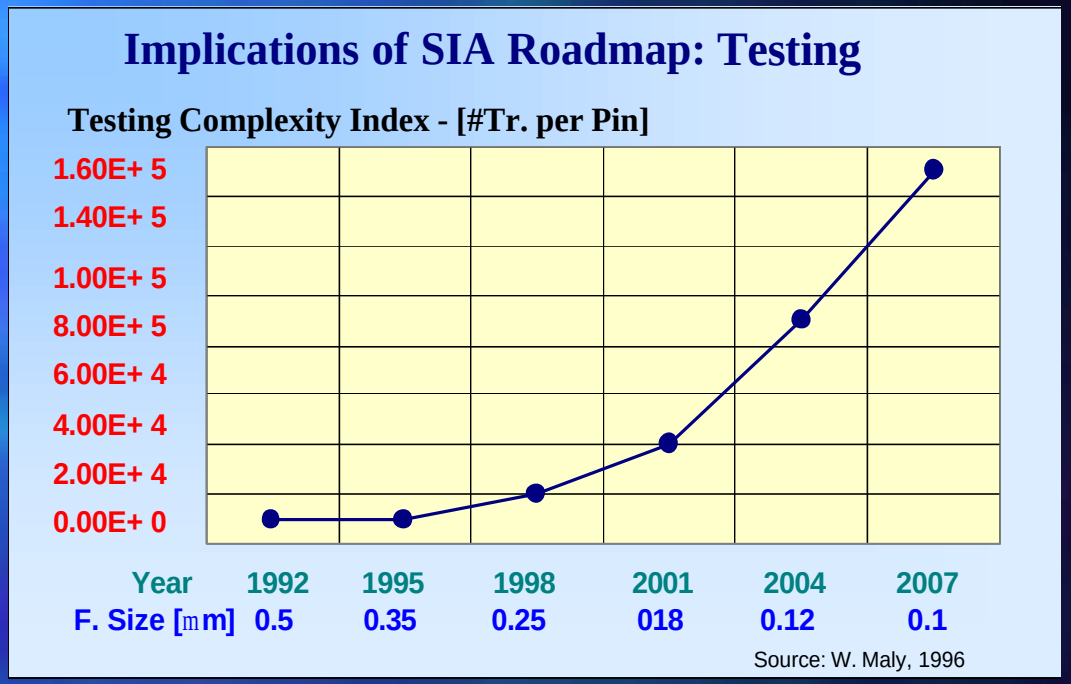
Emerging New Challenges

- Observe Implications on Product Realization
- Analyze Existing Quality Assurance Approaches
- Identify Challenges
- Demonstrate Potential Solutions

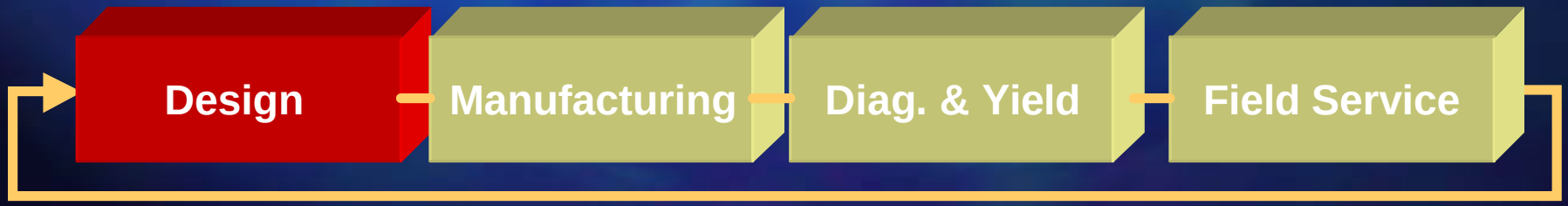


Design Challenge: Quality

- Implication:
  - # of Transistors per pin (Testing Complexity Index)
  - increased internal speed vs external

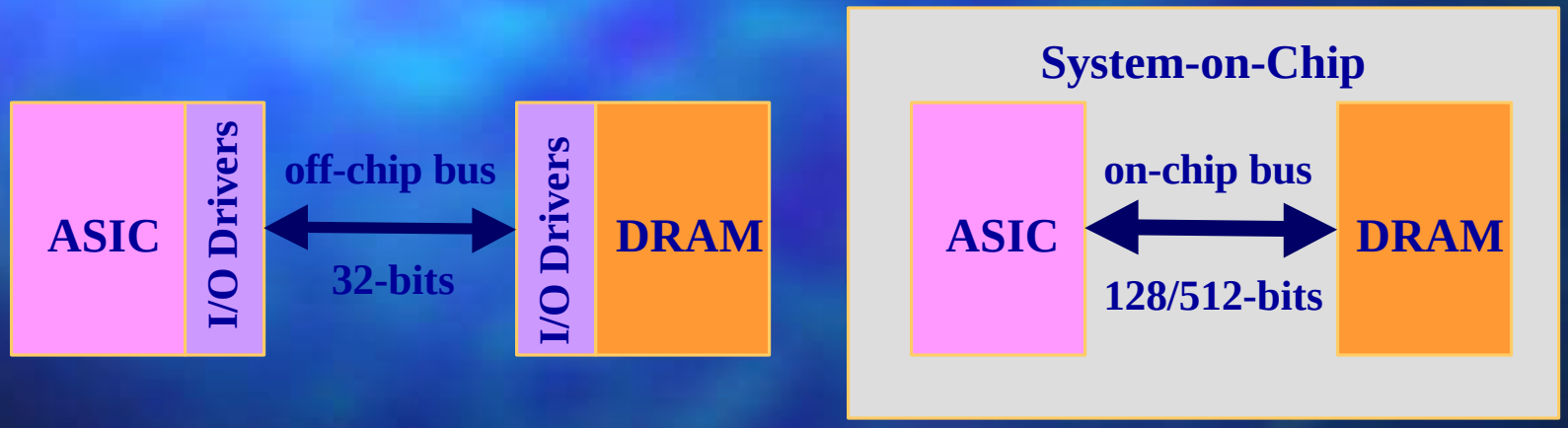


Source: SIA Roadma



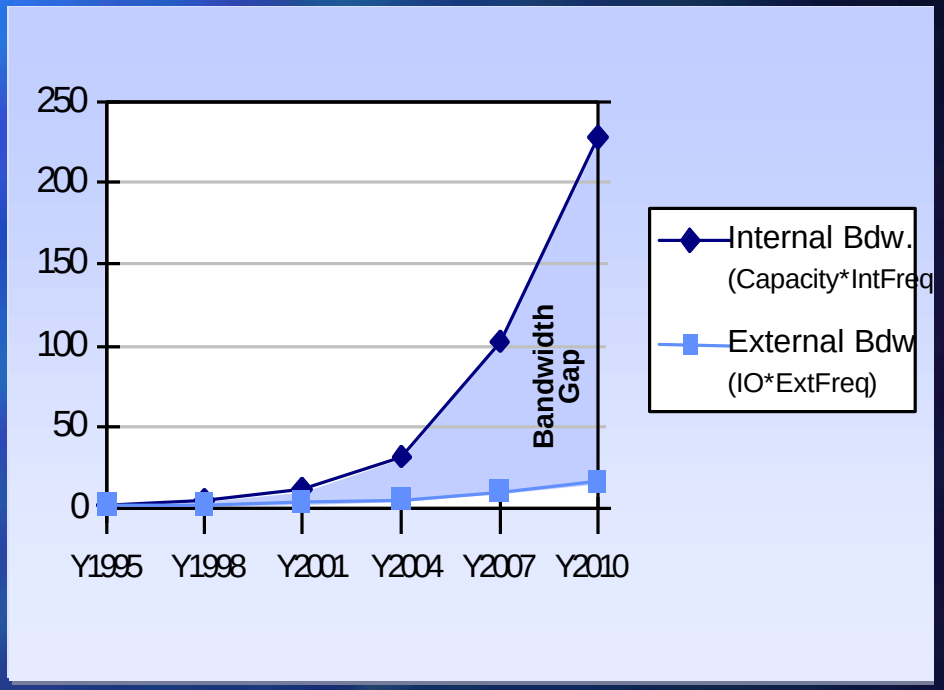
Design Challenge: Quality

- Leverage Internal Bandwidth vs External Bandwidth



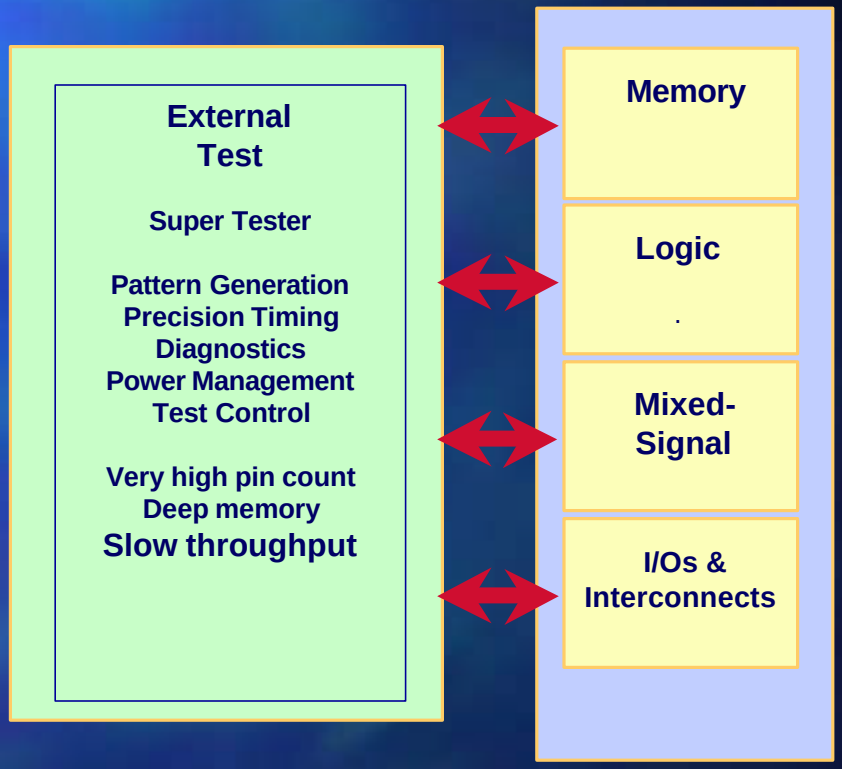
Design Challenge: Quality

- External Bandwidth
  - max bits of data/time from ATE to IC
- Internal Bandwidth
  max bits of data/time from on-chip test resource to embedded core
- Bandwidth Gap



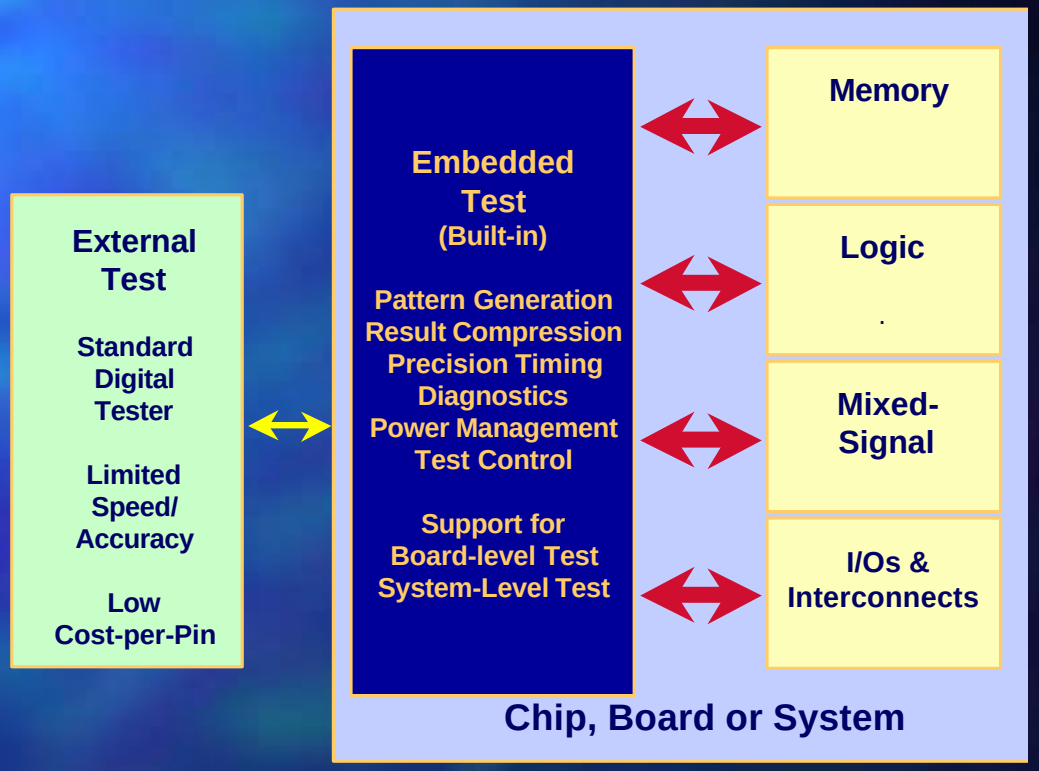
Design Challenge: Quality

- External Test Data Volume can be extremely high (function of chip complexity)
- Requires deep tester memory for scan I/O pins
- Slow test throughput with long scan chains, especially for core-based designs



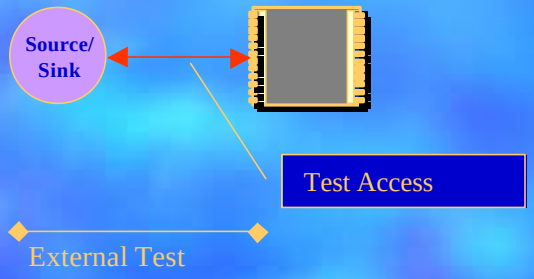
Design Challenge: Quality

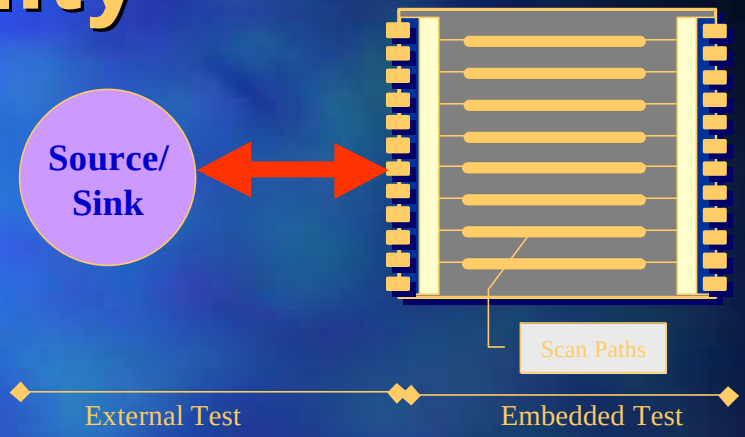
- Solution: Dedicated Built-In H/W for embedded test functions
- Repartition tester into embedded test and external test functions
- Include low H/W cost and high data volume embedded-quality for test

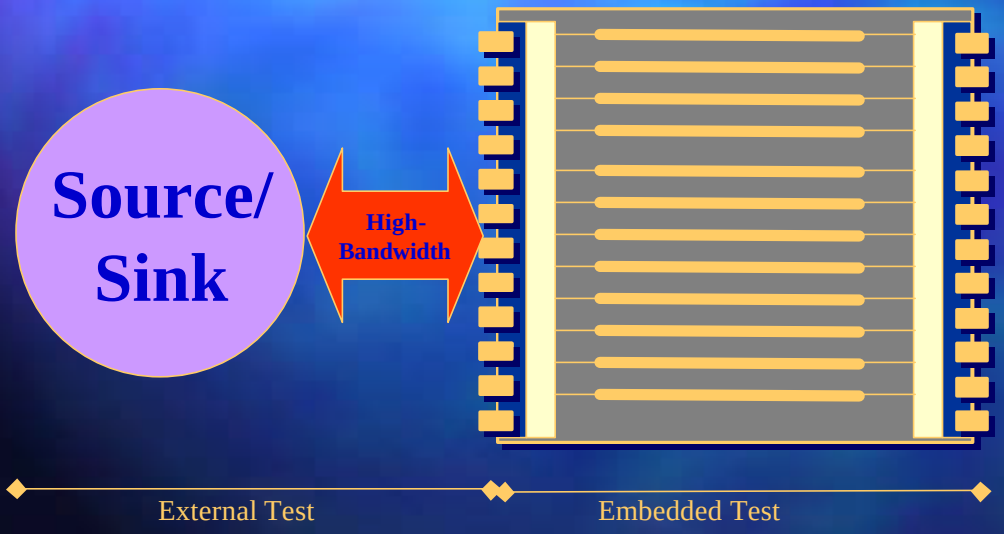


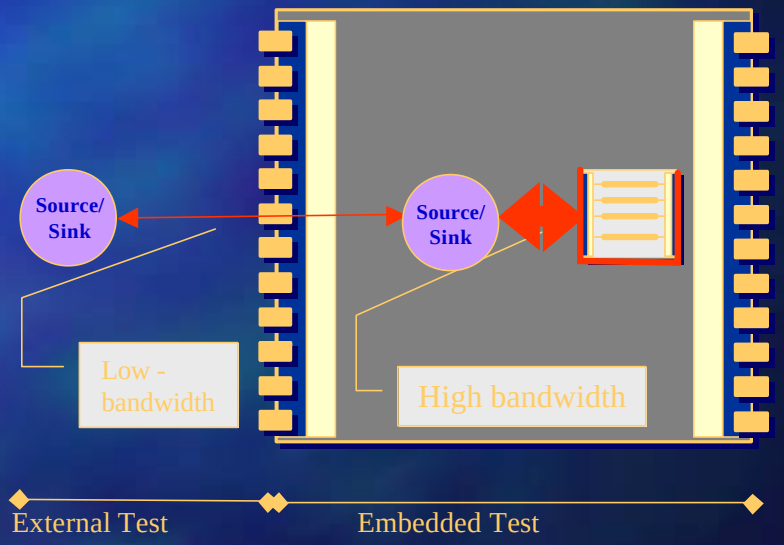
Source: LogicVision

Design Challenge: Quality



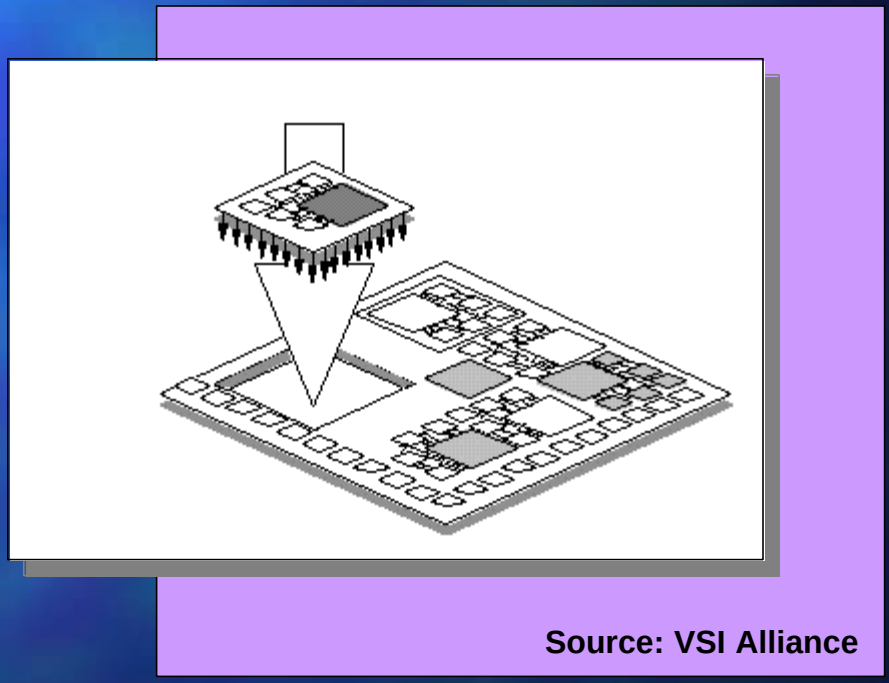






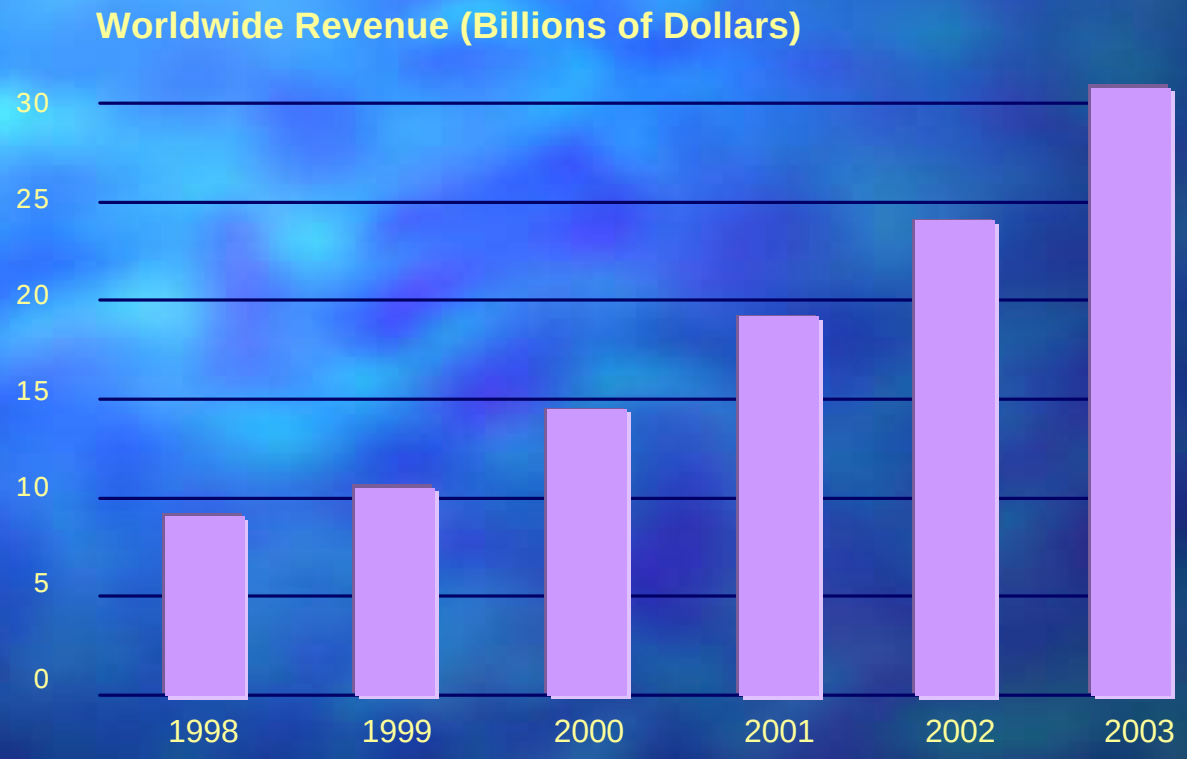
Design Challenge: TTM

- Implication: Emergence of reusable core-based design
- Multiple hardware description levels (hard, soft, firm)
- Standard IC functions (library elements) and legacy cores



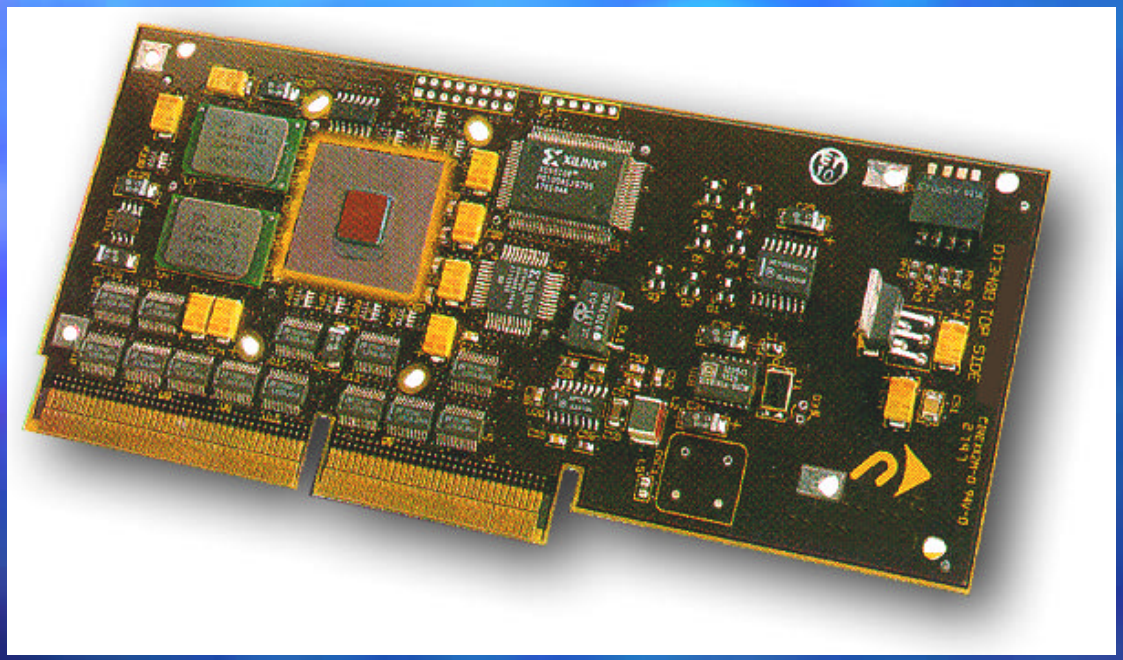
Source: VSI Alliance

SOC Market Growth



Source: Dataquest

Paradigm Shift in SOC Design

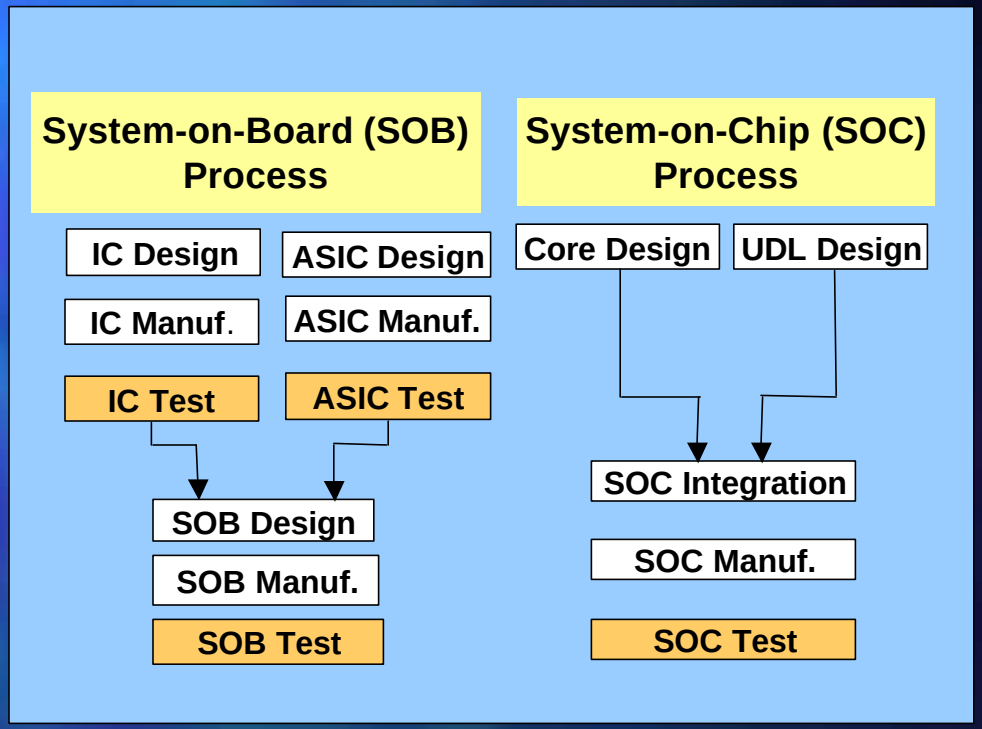


System on a board

System on a Chip

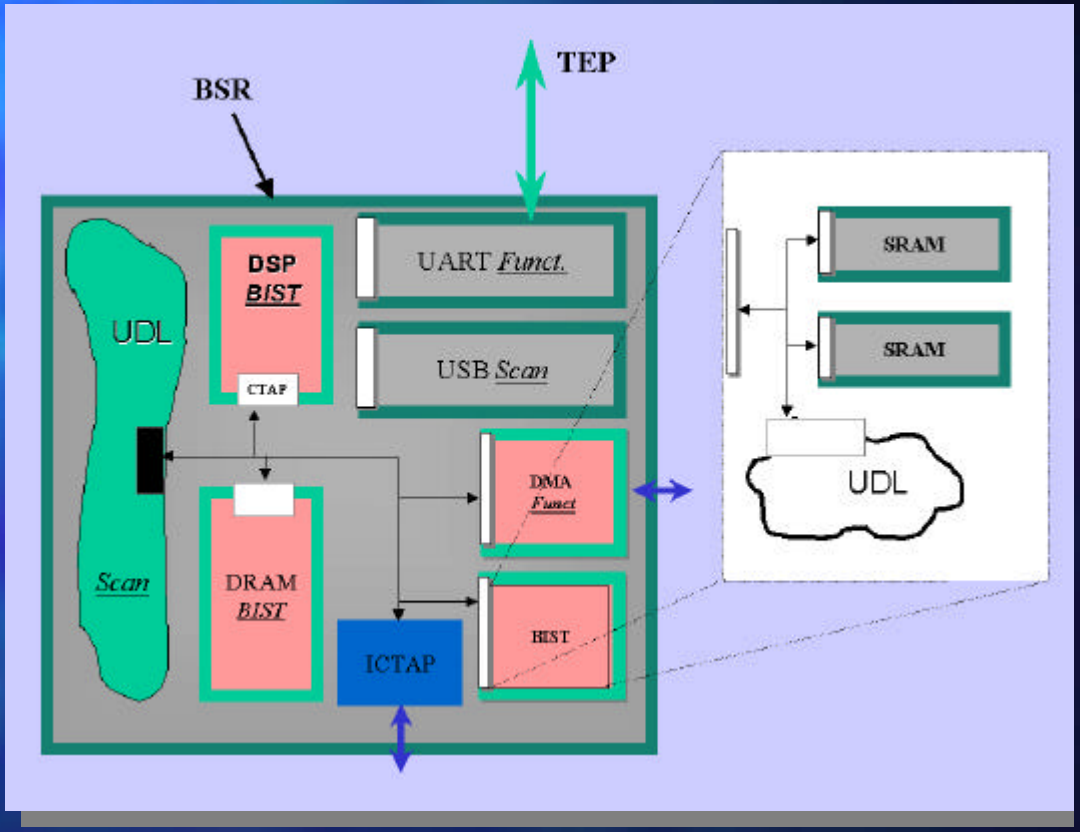
Design Challenge: TTM

- SOC manufactured and tested in single stage
- Core I/Os often more than Chip I/Os
- Test generation difficult due to limited core design knowledge
- Direct access to core ports unavailable
- Core & UDL test part of System-On-Chip test



Design Challenge: TTM

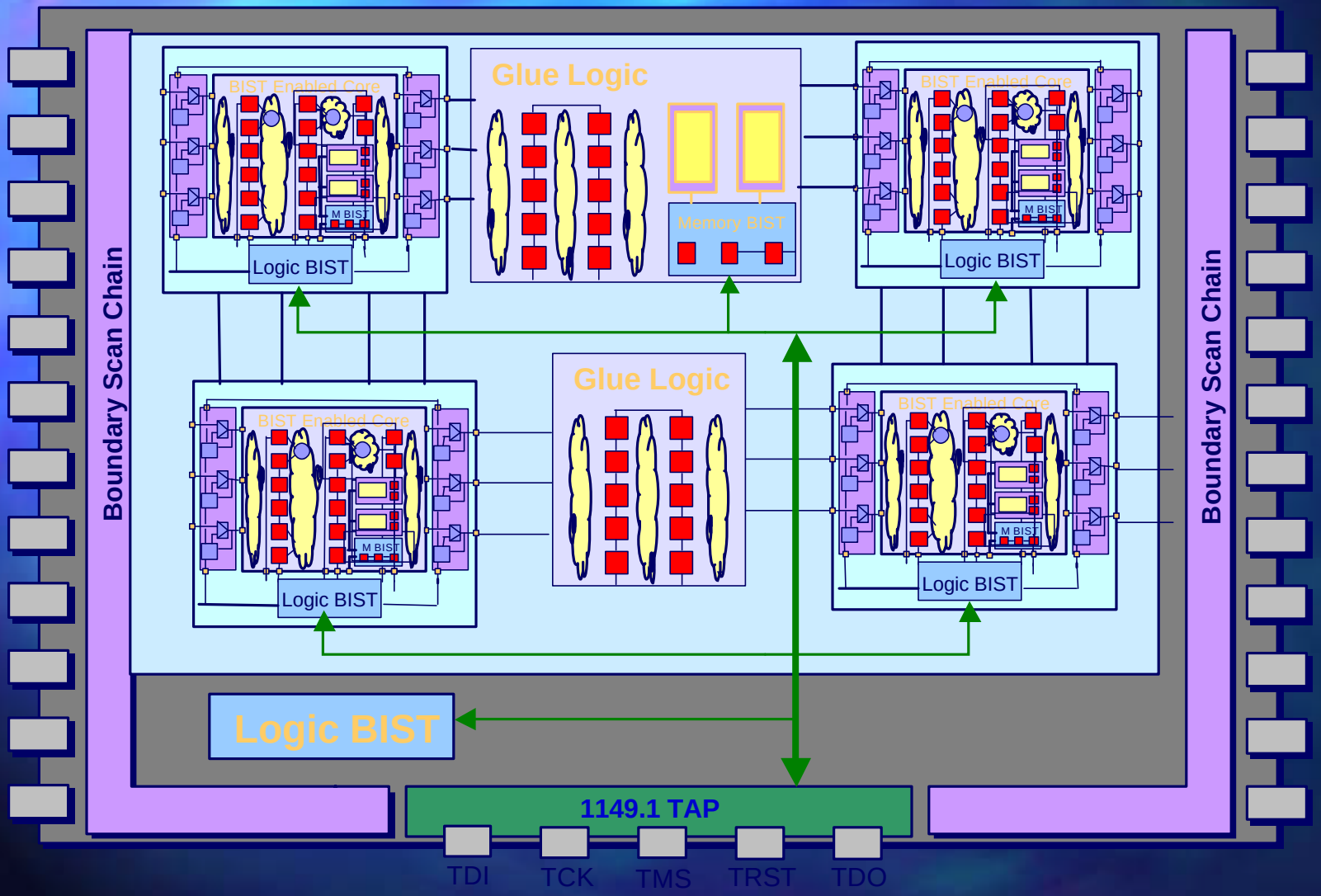
- Built-in dedicated H/W to create autonomous internal core test
- Built-in dedicate System-On-Chip test optimization
- Built-In standard core test interface for each core



Design Challenge: TTM

- IEEE P1500 (9/96) develops a standard for embedded core test interface comprised of:
  - Standard Core Test Information Model (CTL) using a Standard Description Language (STIL)
  - Standard Core Test Wrapper and Control Mechanism
  - Phase 1: Dual Compliance for Digital Cores (1149.1)
  - Phase 2: Analog Cores (1149.4), Testability Guidelines
- VSI Manufacturing Test Related DWG supports IEEE P1500 standardization

Design Challenge: TTM

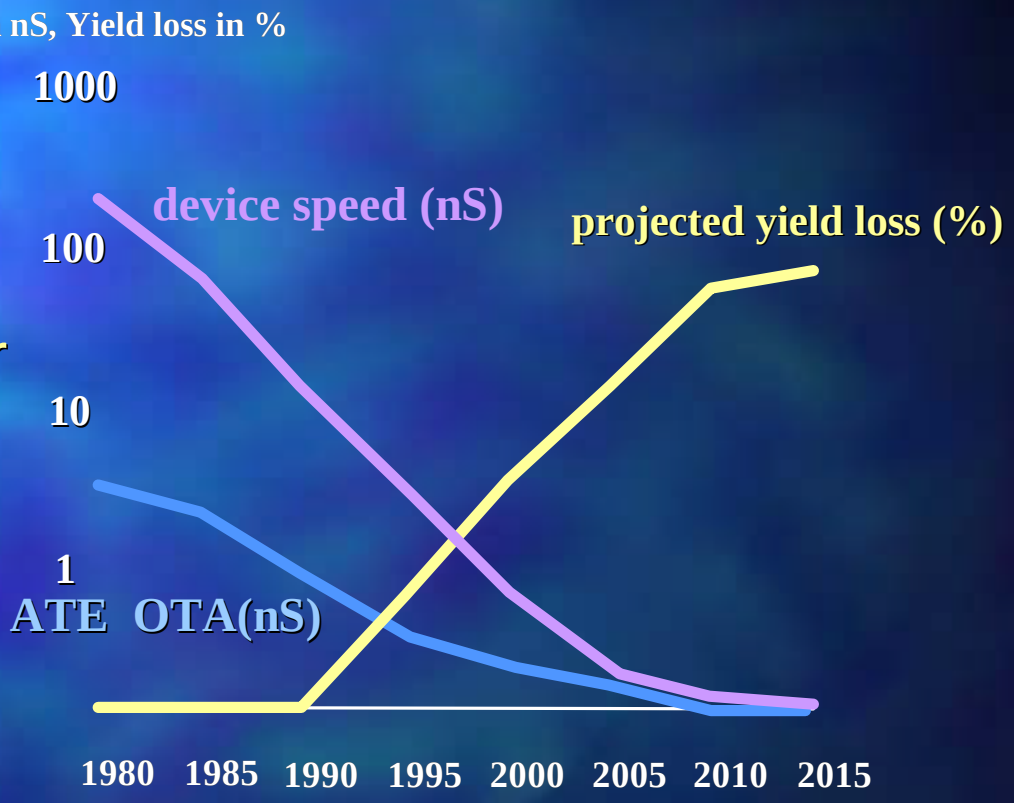


Design Challenge: Quality

- Implication: Increased chip internal speed
  (ASSP with 200MHz+, Microprocessors with 1 GHz+)
  - Multiple and overlapping clock domains
  - Multi-cycle data paths
  - Complex clock distribution
- Recent SEMATECH study revealed criticality of performance faults

Design Challenge: Quality

- High speed ATE substantially more expensive
- ATE vs Chip Technology discrepancy: Tester uses 5 year old technology - chips move to next generation every 2 years
- ATE accuracy degrading: Chip cycle time will crossover ATE accuracy



Design Challenge: Quality

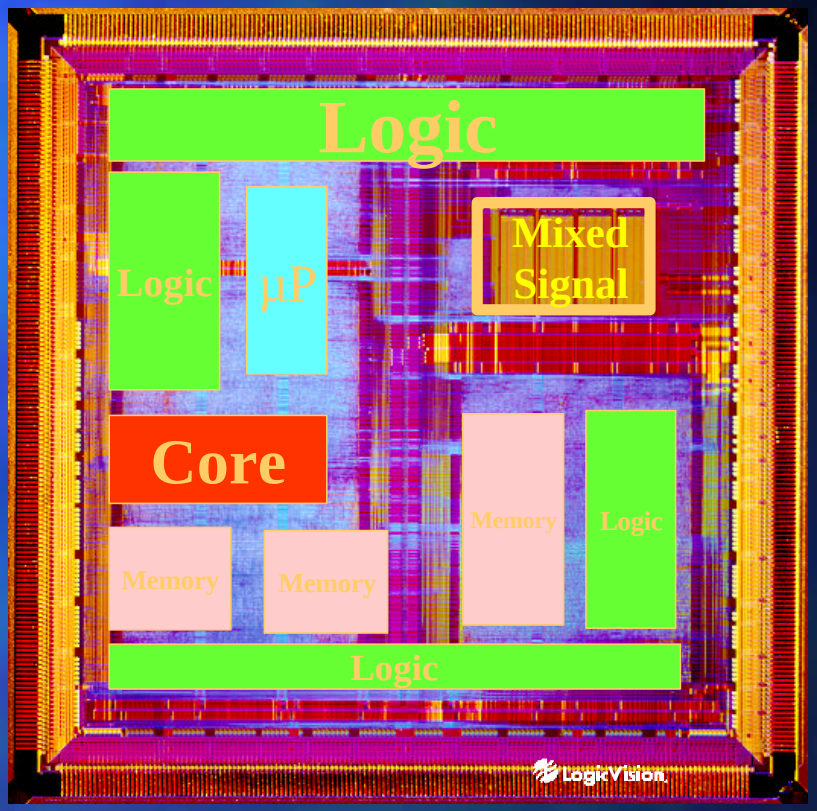
- Solution: Built-In dedicated H/W to run Built-In Self-Test at-speed and detect performance faults

- Major move for mainstream systems to implement at-speed BIST for production test

Source: Sun Microsystems

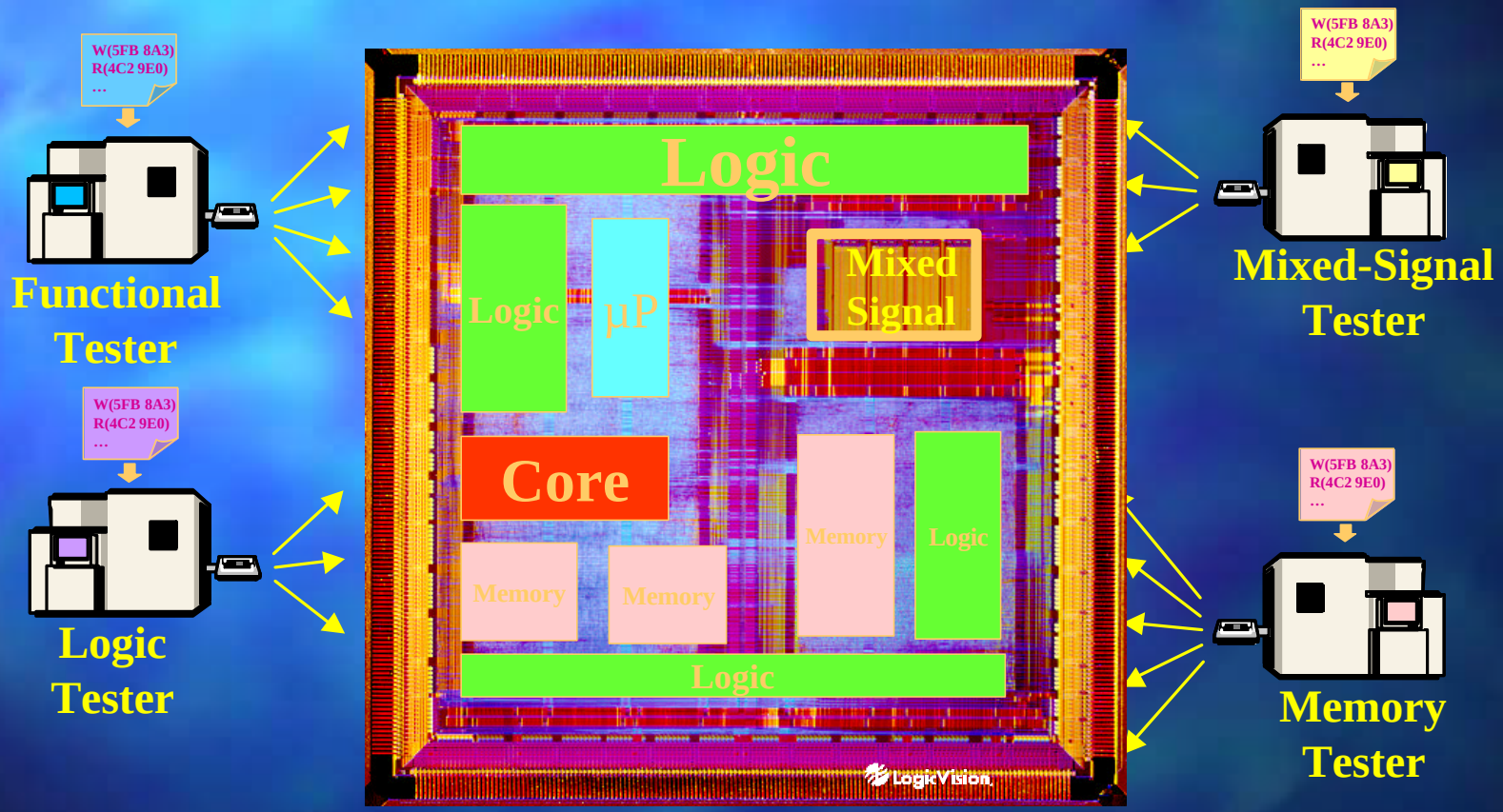
Manufacturing Challenge: Test Cost

- Embed in a single chip: Logic, Analog, DRAM blocks
- Embed advanced technology blocks:
  - FPGA, Flash, RF/Microwave
- Beyond Electronic blocks:
  - MEMS
  - Optical elements



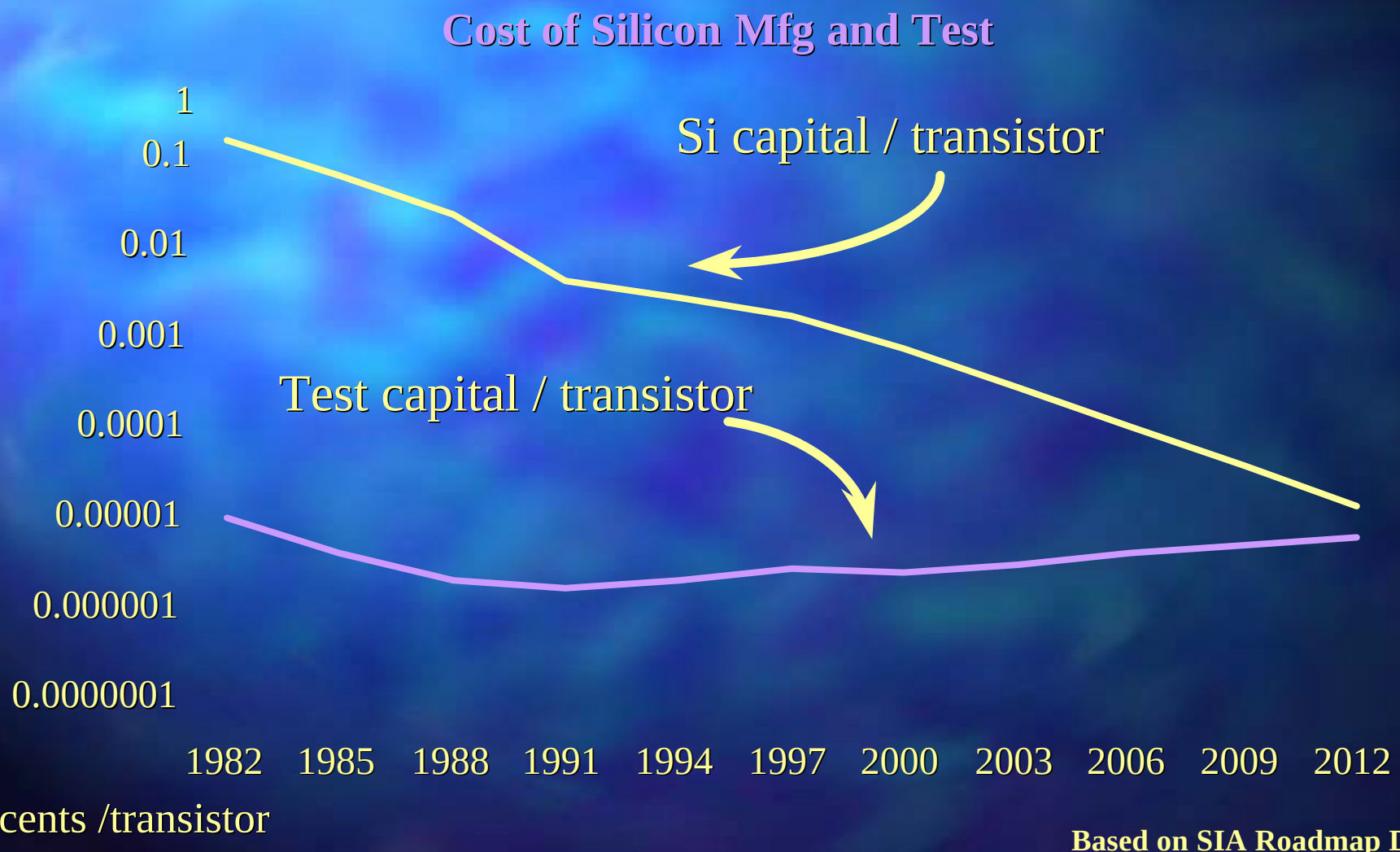
Design → Manufacturing → Diag. & Yield → Field Service

Manufacturing Challenge: Test Cost



Multiple Insertions or Super ATE!

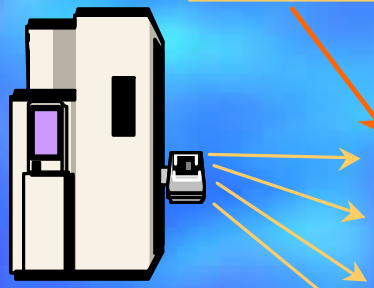
Moore's Law for Test



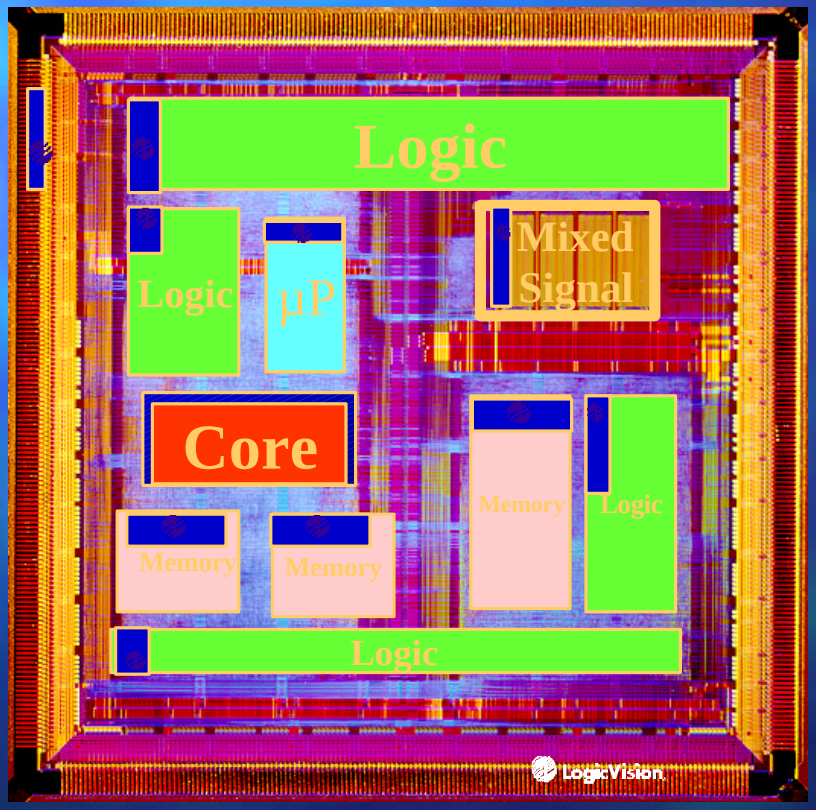
Based on SIA Roadmap Data

Manufacturing Challenge: Test Cost

JTAG 4 Pin Interface



Low Cost Sort Machine with
gicVision BIST Access Software



I/O's tri-stated
no critical
timing

If full scan already exists
hen the dues are already paid

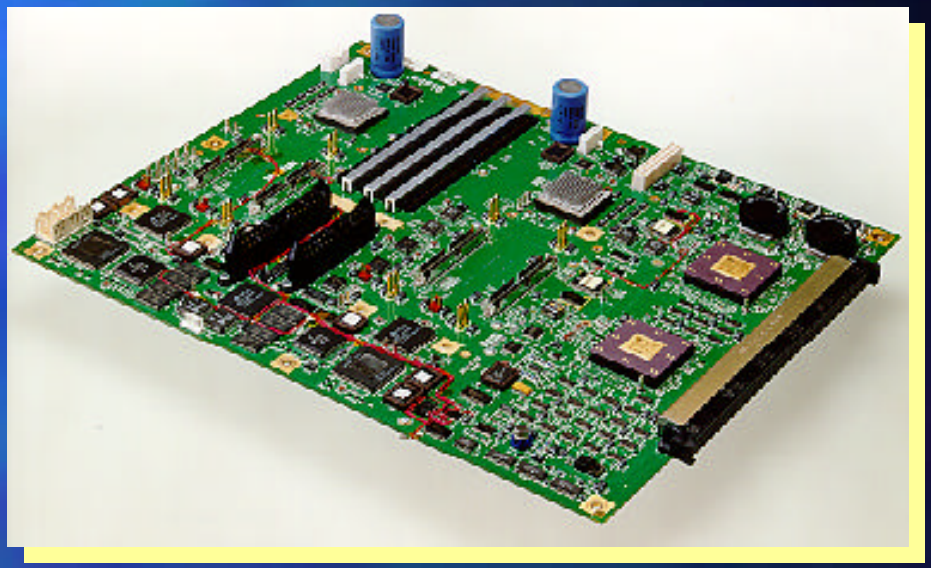
LogicVision's Embedded Test

Manufacturing Challenge: Quality

- High Density Chips: Advanced Semiconductor Technology with very high density
  - number of millions of transistors per sq. cm. will increase by a factor of three in next five years
  - Test Escape due to unmodeled faults (ex: SOI process, Copper Interconnect)
  - Use built-In dedicated h/w to execute fault model independent pseudo-random pattern based test

Manufacturing Challenge: Quality

- Challenge: High performance board and MCM applications (ex: 500MHz chip-to-chip)
- Require Chip-to-Chip Interconnect test for static and dynamic faults

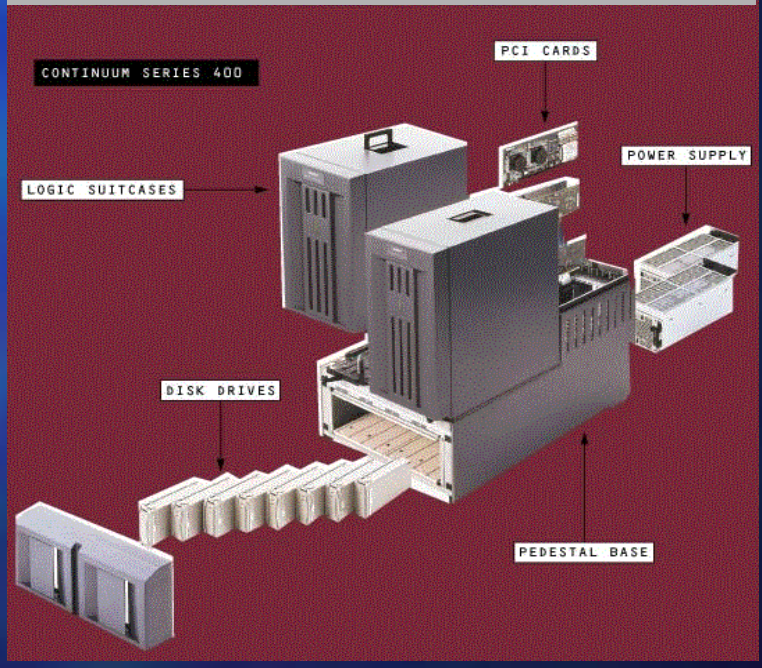


Source: Stratus Computers

Manufacturing Challenge: Quality

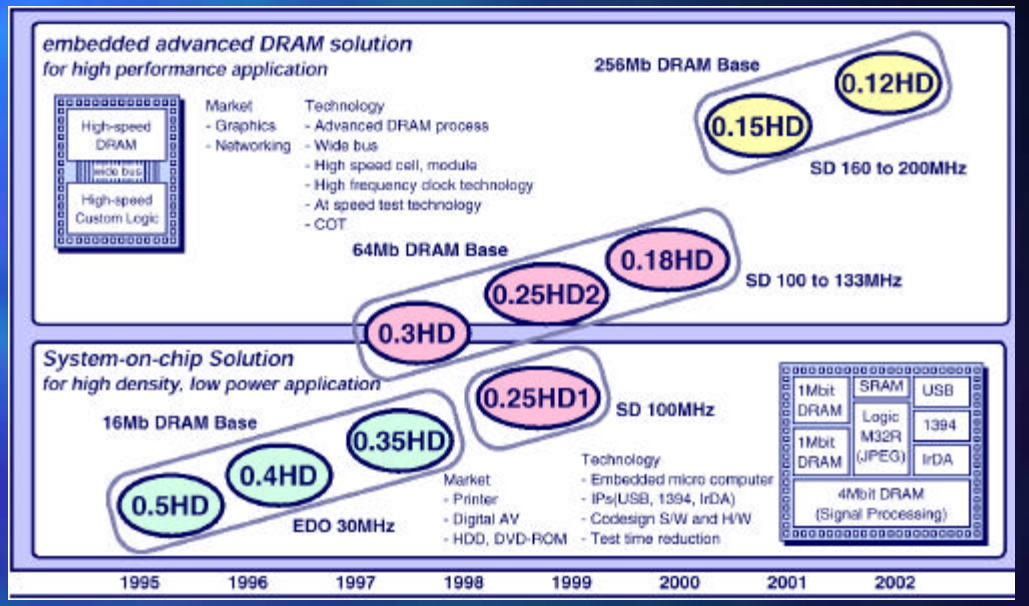
- Solution:
  - IEEE 1149.1 Boundary-Scan for static faults
  - At-Speed Interconnect Test requires Built-In dedicated H/W

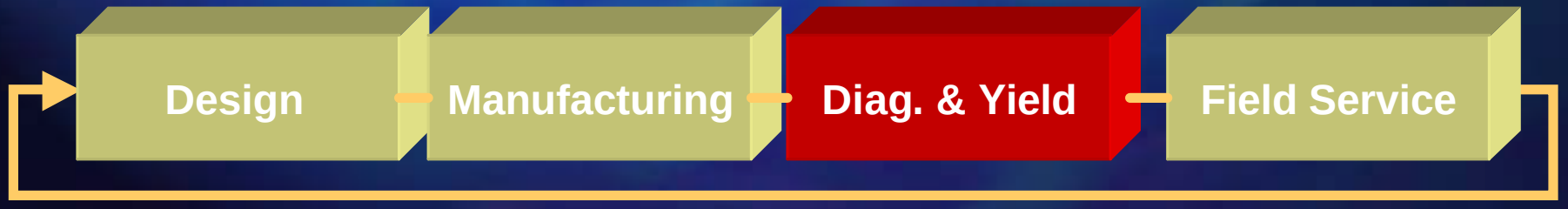
Source: Stratus Computers



Diagnosis & Yield Challenge: Cost

- Implication: Large Embedded: SRAM, DRAM, Flash
- Beyond certain size memories necessitate redundancy/repair during manufacturing test (and field reliability)
- Requires Logic ATE, Memory ATE, Laser Repair Equipment, and Redundancy Analysis



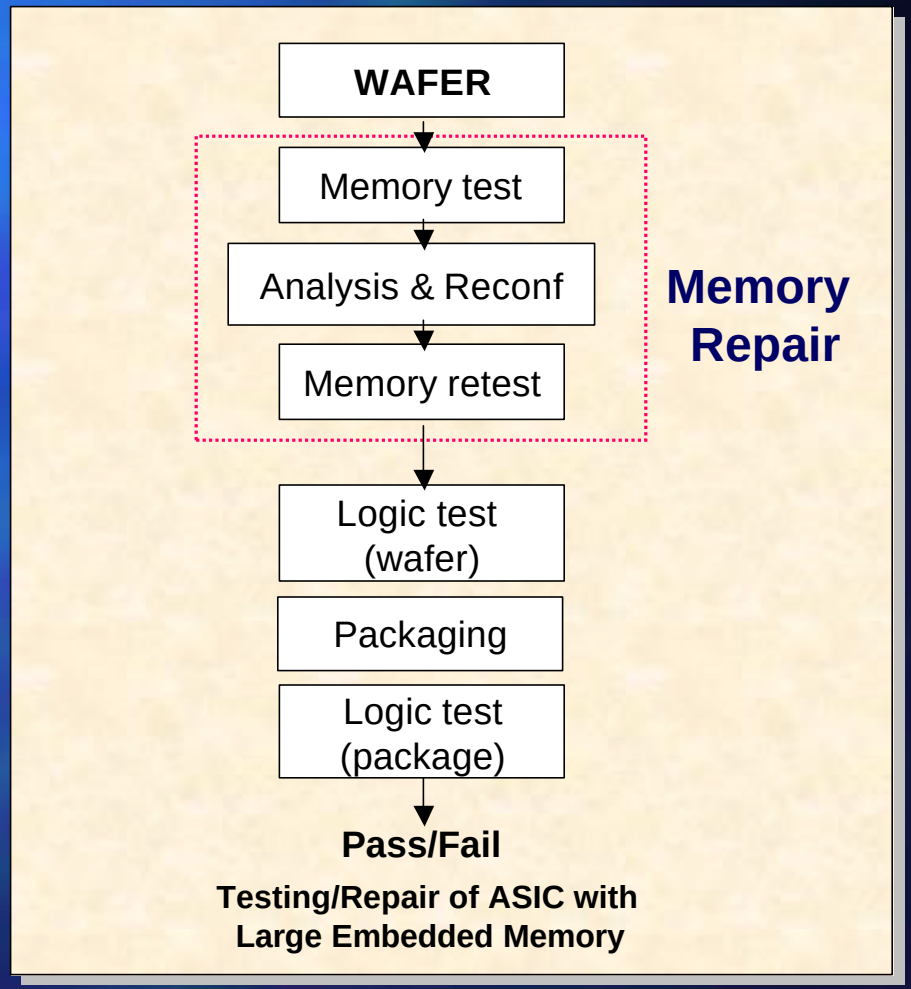


Diagnosis & Yield Challenge: Cost

- Two reconfiguration strategies:

1. Hard: Built-in dedicated h/w for Redundancy Analysis and external repair (fuse blow)
2. Soft: Built-In dedicated reconfiguration mechanism using BISR (test repeatability)

- Adopted by several chip manufacturers

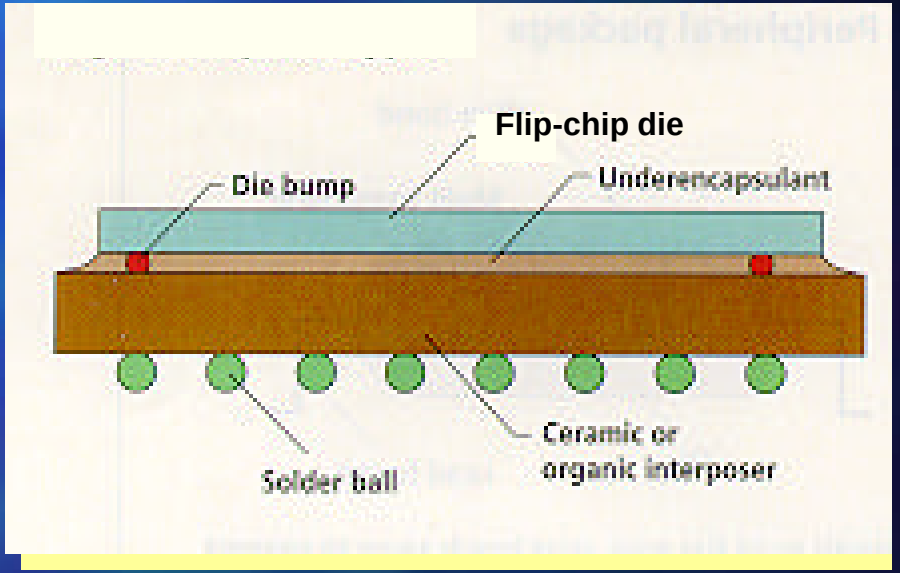


Diagnosis & Yield Challenge: TTM

- Advanced Packaging Technologies
  - Increased use of Flip-Chip Technology: Flip-Chip design dedicates a metal layer for area array interconnects (Direct Chip Attach, Chip Scale Packaging, BGA and MCM)
  - Increased use of Fine-Pitch Technology: probing limitations due to miniaturized package technologies (FC, CSP) -> very expensive probe cards
  - Increased use of bare die usage -> inadequacy of conventional package test (Direct Chip Attach, MCM)

Diagnosis & Yield Challenge: TTM

- Conventional failure mode analysis based on E-beam can not be used with flip-chip
- Solution: Use Embedded Quality functions for diagnosis: stop-on-error, data logging for memories, and scan-based diagnosis for random logic. This can be leveraged for interactive at-speed diagnosis.



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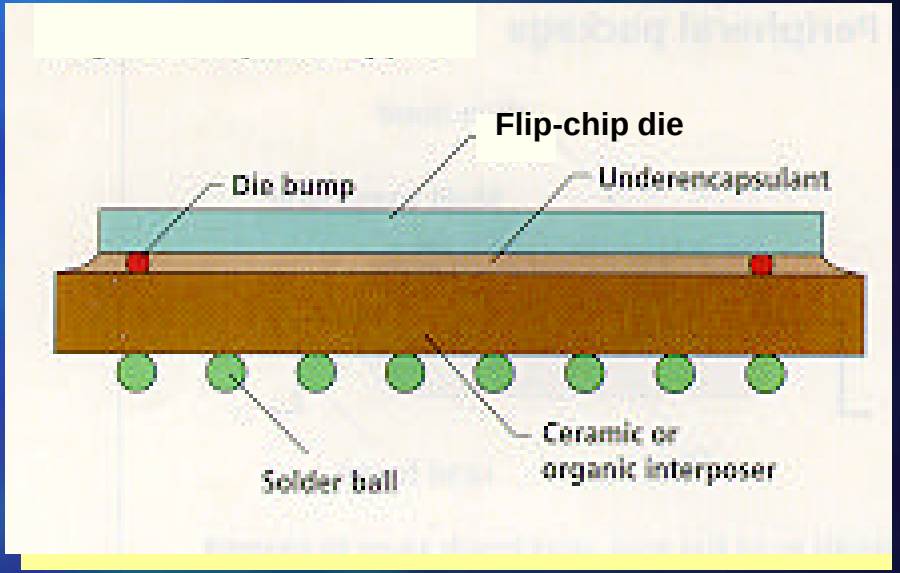
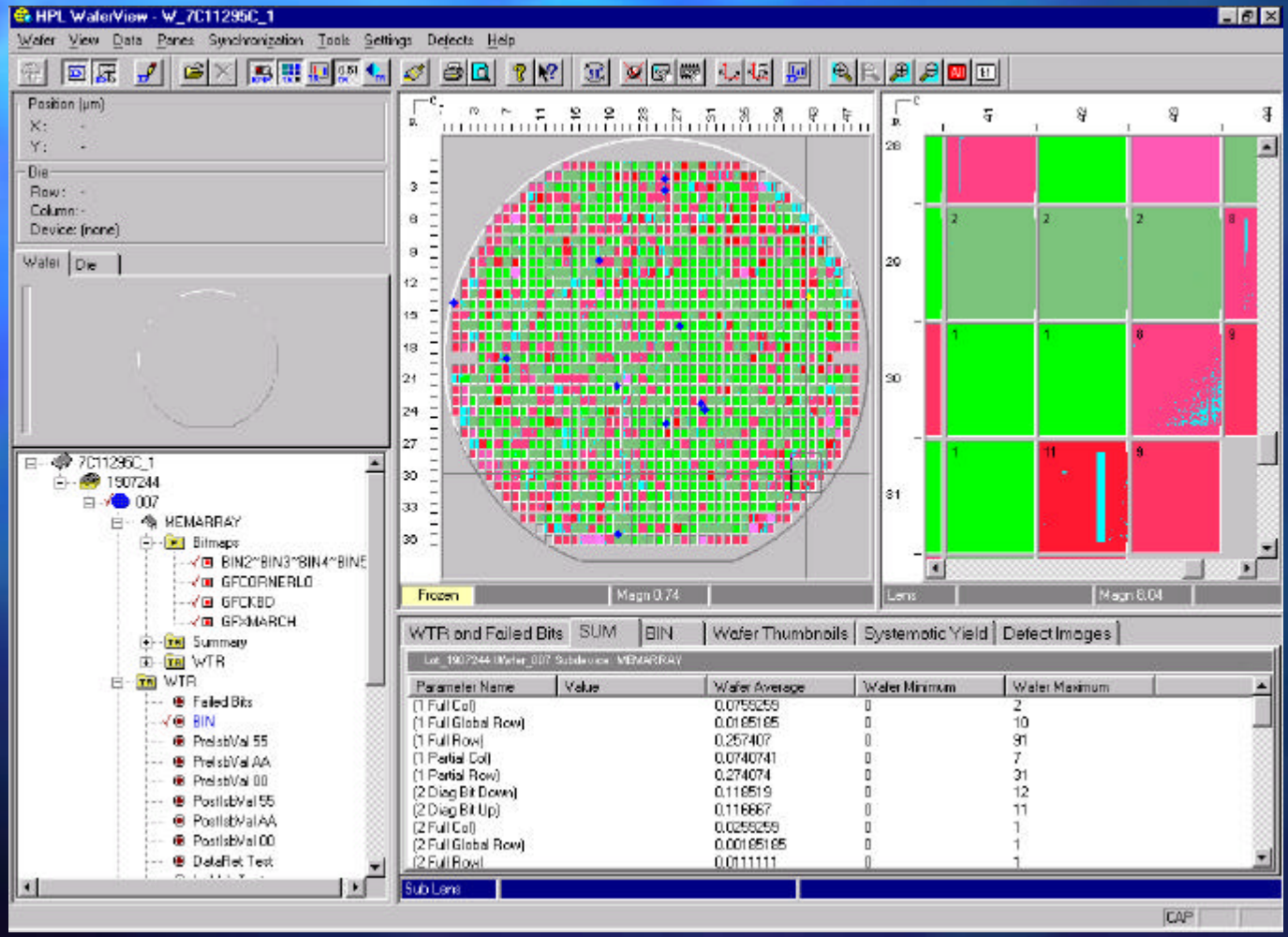
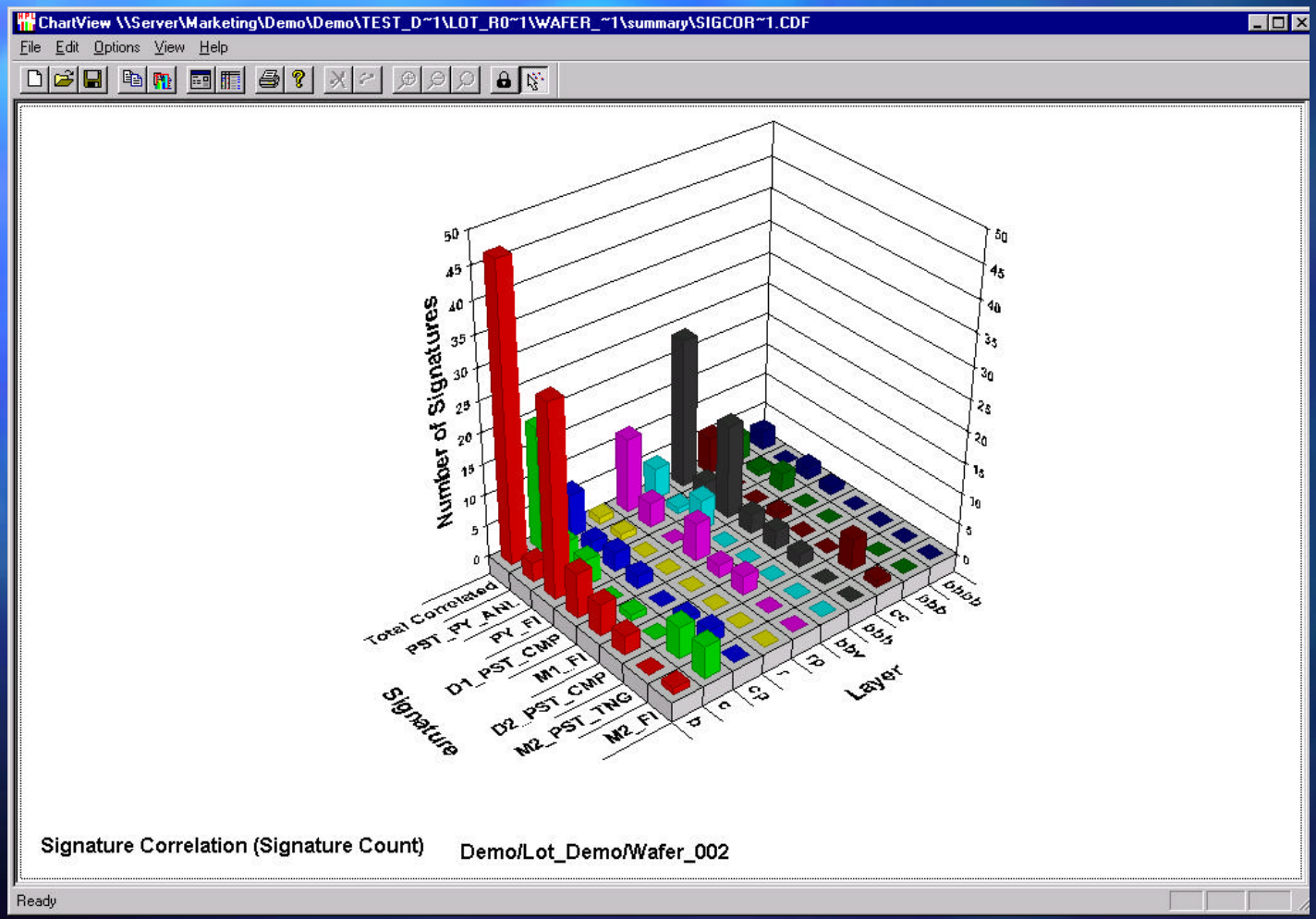


Diagnosis & Yield Challenge: TTM



–Source HPL, Inc

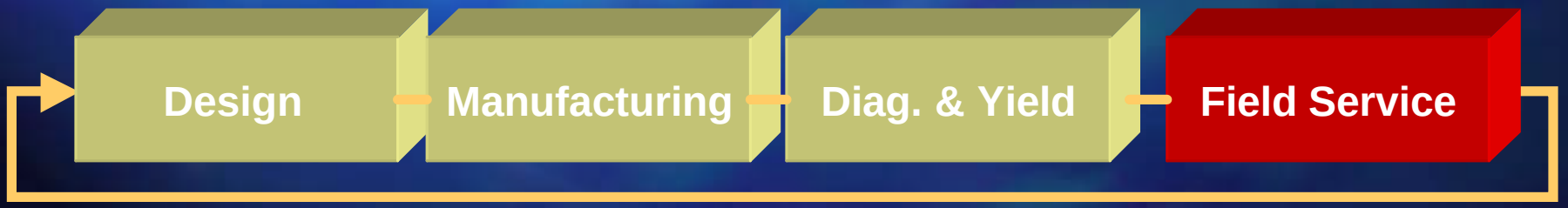
Diagnosis & Yield Challenge: TTM



–Source HPL, In

Field Challenge: Quality

- Challenge: Increase Impact of Cosmic Radiation on Sea Level
- Solutions: Embedded test dedicated h/w function for On-line BIST to detect transient (soft) errors



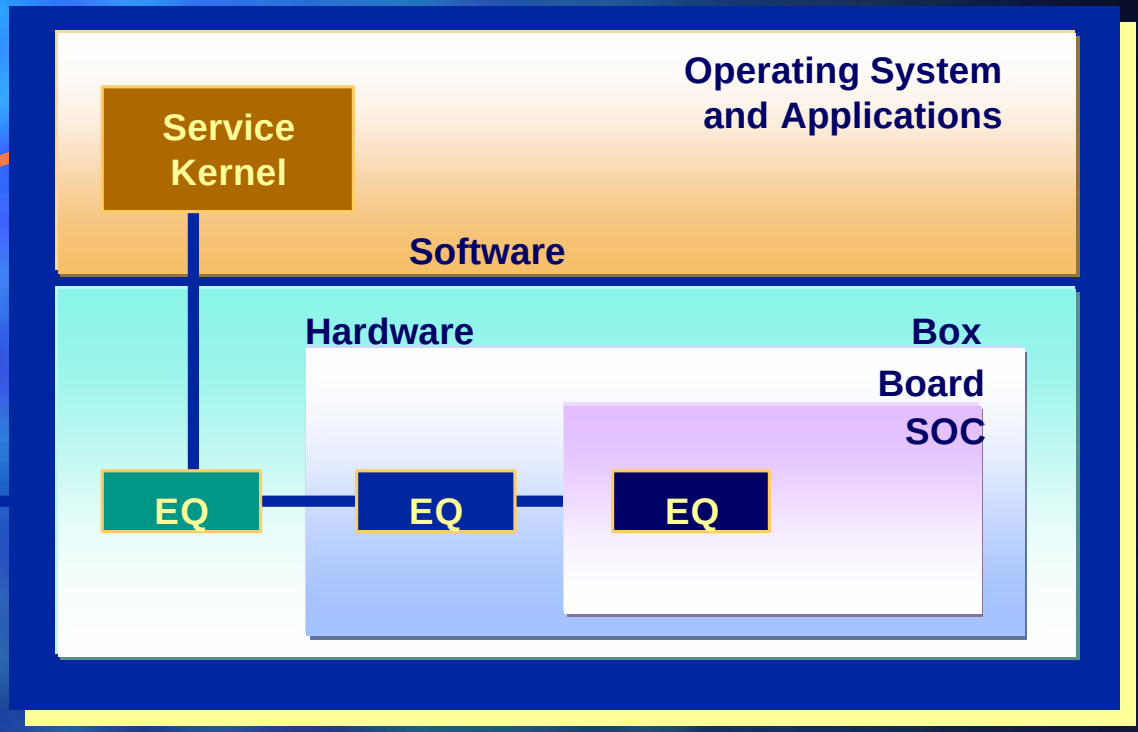
Field Challenge: Cost, TTM

- Design and Manufacturing of Complex Boards and Systems costs too much and takes too long
- Test development cost is 35% of total product development time
- Test, Diagnosis and Repair cost for complex systems reaches 40-50% of total product realization cost

Hierarchical Embedded Test

OS / Software Interface
(accessible by network)
at the Application layer

ATE / Hardware Interface
(accessible by connector)
for Manufacturing or Field

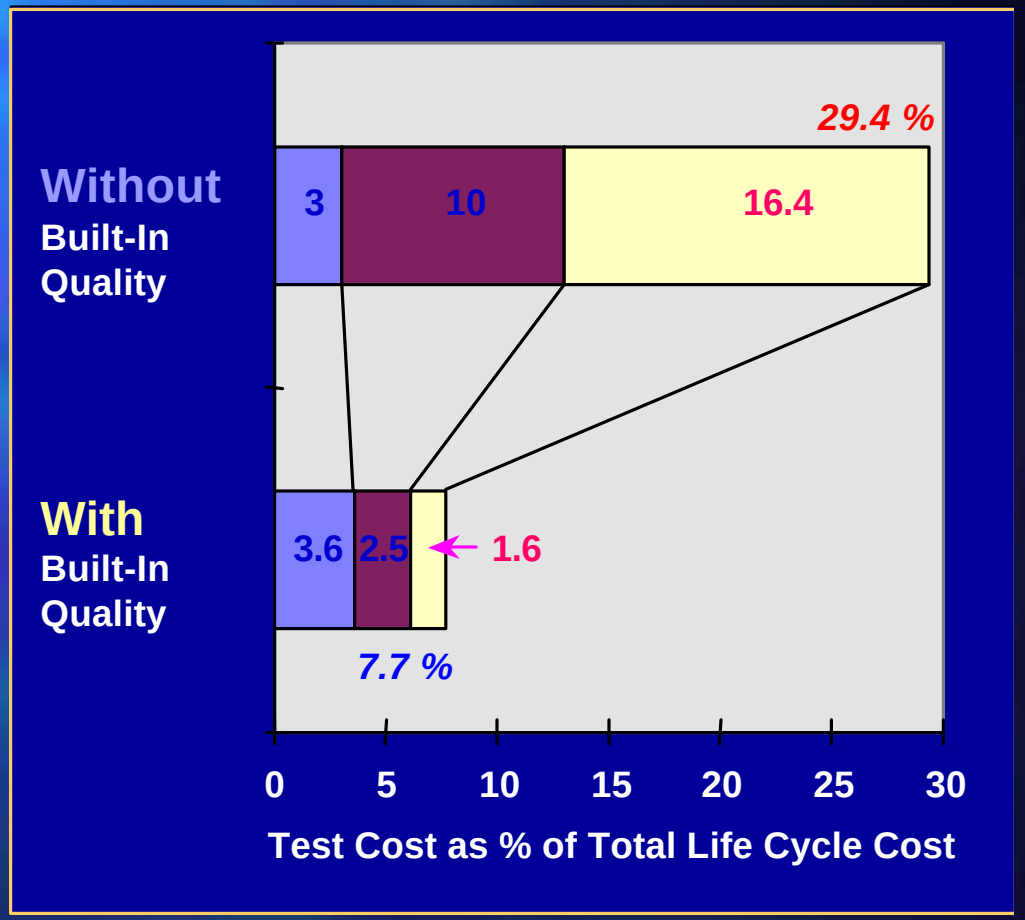


Source:
LogicVision

Reuse of dedicated built-in quality hardware

Field Challenge: Cost, TTM

- Leveraging dedicated Embedded Quality function drastically reduces test development interval and test costs



Source: AeroSpace Study

Conventional Quality Paradox

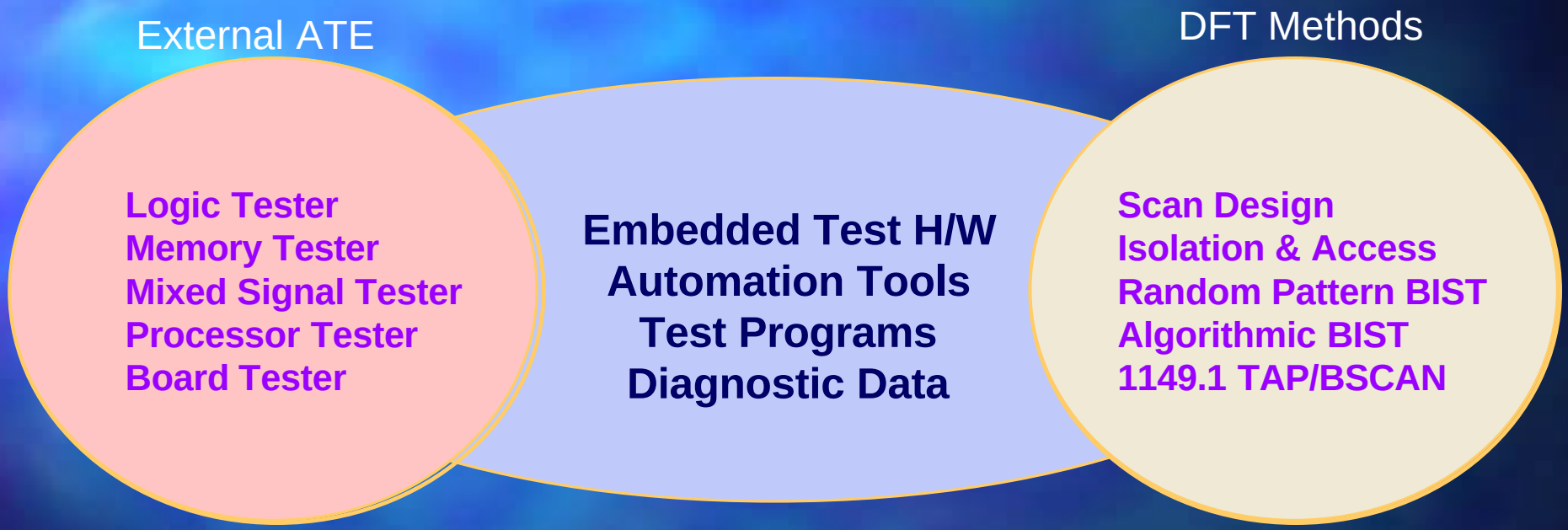
Design Test Management

“It is really not my problem, but I will do what I can to help out.”

Manufacturing Test Management

“I have little control on the design process! I will buy the best testers possible and perform as much testing as possible to ensure the expected quality.”

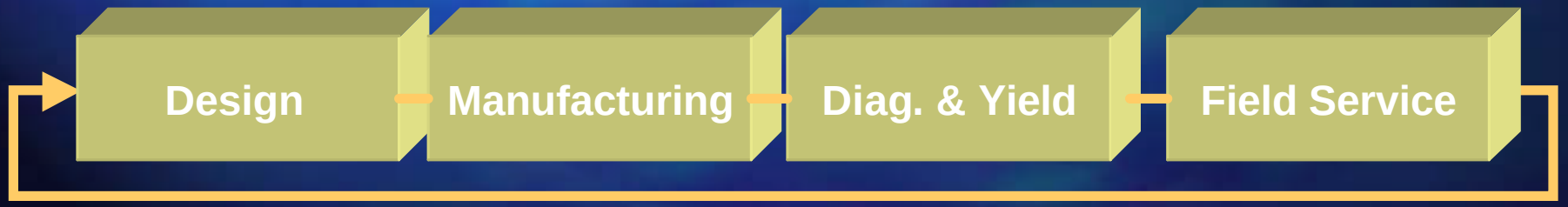
Test Resource Partitioning



A Solution that Combines the Best of DFT and ATE

Conclusions

- To ensure quality of electronic products using emerging technologies:
  - Embedded Quality functions are added into the high level designs of embedded cores, SOCs, board and systems
- A range of Embedded Quality functions provide adequate test, verification, diagnosis, debug, measurement and repair



Thank YOU

for your attention