Call for Papers

ISQED 2016
17th International Symposium & Exhibits on
QUALITY ELECTRONIC DESIGN

ISQED Symposium 2016

www.ISQED.org

IEEE | Electron Devices Society | CAS | Reliability Society

March 2016. Santa Clara, CA, USA

The 17th International Symposium on Quality Electronic Design (ISQED 2016) is the leading Electronic IC and System Design conference, aimed at bridging the gap among electronic design tools and processes, integrated circuit technologies, processes & manufacturing, to achieve design quality. ISQED is the pioneer and leading international conference dealing with design for manufacturability and quality issues front-to-back. ISQED emphasizes a holistic approach toward electronic design and intends to highlight and accelerate cooperation among the IC & System Design, EDA, Semiconductor Process Technology and Manufacturing communities. ISQED spans three days, Monday through Wednesday, in three parallel tracks, hosting over 100 peer-reviewed technical presentations, several keynote speakers, workshops/tutorials and other informal meetings. Past conference proceedings and papers have been published in the IEEE Xplore digital library and indexed by SCOPUS. For any question please contact the publication committee by sending email to isqed2016@isqed.org.

Papers are accepted in the following areas

A pioneer and leading multidisciplinary conference, ISQED accepts and promotes papers in the following areas:

Cognitive Computing in Hardware (CCH)
Hardware accelerators for machine learning and deep learning algorithms including Support Vector Machines, Neural Networks, Hidden Markov Model Decoding, and Genetic Algorithms. Machine learning algorithms optimized for CPUs or general purpose GPUs (GPGPUs). FPGA-accelerated implementations of machine learning algorithms. Hardware implementations of machine learning algorithms for applications like image/object recognition, computer vision, speech recognition, and natural language processing. Machine-learning based intelligence in IoT under highly constrained energy/power requirements. System-wide partitioning for deep learning algorithms: algorithm training and recognition from cloud/server to IoT node.

Hardware and System Security (HSS)
Hardware security attacks including (but not limited to) side-channel attacks, reverse engineering, tampering, and Trojans. Supply-chain integrity. Security for memory technologies. Hardware-based security primitives including PUFs, TRNGs, and ciphers. Design of encryption circuits. Security, privacy, trust protocols, and trusted information flow using hardware security primitives. Trusted design automation using untrusted tools. Trusted manufacturing including split manufacturing, remote IC enabling/disabling, watermarking, and fingerprinting. Techniques and metrics for hardware/software usage metering; evaluating system-data/hardware-design confidentiality, integrity, and authenticity; and, ensuring system security.

Design Technology Co-Optimization (DTCO)
Optimization-based methodologies that address the interaction between design (custom, semi-custom, ASIC, FPGA, RF, memory, etc.) and advanced node manufacturing techniques such as multiple patterning, EUV lithography, DSA lithography, and advanced interconnect (e.g., air gap for local interconnect, Si photonics, etc.). Modeling, analysis, and optimization of technology implications on performance metrics like power consumption, timing, area, and cost. Design methods and tools to improve yield and manufacturability.

Design Verification and Design for Testability (DVFT)
Hardware and software formal-, assertion-, and simulation-based design verification techniques to ensure the functional correctness of hardware early in the design cycle. DFT and BIST for digital designs, analog/mixed-signal IC's, SoC's, and memories. Test synthesis and synthesis for testability. DFT economics, DFT case studies. DFT and ATE. Fault diagnosis, IDDQ test, novel test methods, effectiveness of test methods, fault models and ATPG, and DPPM prediction. SoC/IP testing strategies. Design methodologies dealing with the link between testability and manufacturing.

EDA, Physical Design, and IP Cores (EDA)
EDA and physical design tools, processes, methodologies, and flows that address issues such as: large-scale SoC design, low-power design, noise sensitivity reduction, reliable clock distribution, timing closure, parasitic extraction, and reliable power grid design and analysis. Design tools for analysis/ tolerance of variation, aging, and soft-errors. Design and maintenance of hard and soft IP blocks, including methods and tools for analysis, comparison, and qualification of IP blocks. Challenges and solutions of integrating, testing, qualifying and manufacturing IP blocks from multiple vendors. Application of EDA to non-traditional problems such as smart power grid, Solar energy, etc.

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Emerging Process & Device Technologies and Design Issues (EDT)
Emerging processes and device technologies and implications on IC design. Emerging technologies including tunnel FETs, steep switching slope devices, horizontal/vertical nanowires, carbon nanotubes, and other nano-devices. Device design and circuit optimization in emerging non-volatile memory and logic, such as Spin-Transfer Torque RAM, Phase Change Memory, Resistive RAM, and Memristors. Use of emerging devices for cognitive, neuromorphic, or quantum computing. Specialty technologies such as MEMs, CIS co-integration with application processors for the IoT market.

Integrated Circuit Design (ICD)
Low power, high-performance, and robust design of logic, memory, analog, RF, programmable logic, and FPGA circuits. Techniques for leakage control, power optimization, and power management including integrated voltage regulators. Clock-generation and distribution circuits, including all-digital PLLs and DLLs. Low power on-chip and chip-to-chip interconnect solutions. Analog- to-digital and digital-to-analog converters. Adaptive digital circuits and systems. Soft-error and fault-tolerant circuits. Circuit design for reliability effects such as gate oxide integrity, electromigration, ESD, HCI, NBTI, PBTI etc. On-chip process, voltage, temperature, and aging sensors and monitoring.

Smart Sensors for IoT – Design and Technology (SSDT)
Sensor and actuator devices for use in IoT applications like Smart Home/Office automation, robotics, connected vehicles, aircraft, wearable systems, implantable electronics, environmental monitoring, and other industrial uses. Device technologies for sensors including MEMS, magnetic, optical, chemical, and biological. Hardware design for sensors including interface, calibration, energy harvesting, signal processing, and power management. Software design for smart sensors including data processing algorithms and information fusion. Sensor network design and processing.

System-level Design and Methodologies (SDM)
Emerging system-level design paradigms, methods and tools aiming at quality of systems including multi-core processors, graphics processors; embedded systems, SoC, novel accelerator designs, and heterogeneous architecture designs. System-level trade-off analysis and multi-objective (e.g. yield, power, delay, area, etc.) optimization. System level power and thermal management. The influence of nanometer technology issues on the system level design. System level modeling and simulation to characterize effects of process, voltage, temperature, and aging on power, performance, and reliability.

Three Dimensional Integration and Advanced Packaging (TDIP)
Innovative packaging technologies including 3D IC, 2.5D or interposer, and multi-chip module and their impact on system design. Design techniques, methodologies, flows and EDA solutions for vertically integrated circuits/chips such as 2.5D, TSV-based 3D, and monolithic 3D design including novel partitioning, power delivery design, clock tree design, reliable high-frequency signal communication, heatsink/cooling methods, and design-for-yield techniques. Modeling and mitigation of via-to-via and via-to-device interactions for 3D ICs. Design of die-to-die interfaces in 3D/2.5D ICs. Design-for-testability for 3D/2.5D ICs. System-level design issues in 3D/2.5D. Die-package co-design.

Submission of Papers

Paper submission must be done on-line through the conference web site at www.isqed.org. The guidelines for the final paper format are provided on the conference web site. Authors should submit original, unpublished papers along with an abstract of about 200 words. The manuscripts should not exceed SIX (6) pages, should not use smaller than 10pt font size, and must be consistent with the format provided in the www.isqed.org. The manuscripts longer than 6 pages and/or written in less than 10-pt font sizes will not be reviewed. To permit a blind review, do not include name(s) or affiliation(s) of the author(s) on the manuscript and abstract. The complete contact author information needs to be entered separately. The manuscripts identifying the name and/or affiliations of the authors in the submitted manuscript will be rejected without review. Please check the as-printed appearance of your paper before sending your paper. In case of any problems email isqed2016@isqed.org.

Paper Submission Deadline	**Sept. 17, 2015**
Acceptance Notifications	December 5, 2015
Final Camera-Ready paper	January 10, 2016

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