# CONFERENCE AT A GLANCE

| Date | Time | | | | |
|---|---|---|---|---|---|
| **Monday 3/21/05** | 9:00am-5:00pm | **TUTORIALS**<br>**Design of sub-90nm CMOS Circuits and Design Methodologies**<br>**Package-Chip Co-Design – Strategies & Challenges**<br>Room: San Carlos/San Juan | | | |
| | 6:30pm-8:30pm | **Evening Panel Discussion EP1**<br>**IP Creation and Use**<br>**What roadblocks are ahead or it is just clear and bumpy road?** | | | |
| **Tuesday 3/22/05** | 8:30am-10:15am | **PLENARY SESSION 1P**<br>**Keynote Speeches by:**<br>**John Kibarian, Ashok K. Sinha, Joe Sawicki** | | | |
| | 10:15am-10:30am | Morning Break | | | |
| | 10:30am-12:00pm | **Session 1A**<br>Tools and Flows for Quality Design<br>Room: San Carlos | **Session 1B**<br>High Level Power/Noise Reduction Techniques<br>Room: San Juan | **Session 1C**<br>Leakage and Dynamic Power Issues<br>Room: San Martin | **Session 1D**<br>Poster<br>City Foyer |
| | 12:00pm-1:00pm | **ISQED LUNCHEON** (Sponsored by Synopsys)<br>**Committee Recognition Awards**<br>**Best Paper Awards** (Sponsored by Synopsys) | | | |
| | | **IP Quality: A Design, not a Verification Problem**<br>Michael Keating | | | |
| | 1:00pm-3:05pm | **Session 2A**<br>Test Application and Cost Reduction<br>Room: San Carlos | **Session 2B**<br>DFM and Physical Layout<br>Room: San Juan | **Session 2C**<br>Performance and Reliability Analysis for Yield Optimization<br>Room: San Martin | |
| | 3:05pm-3:15pm | Afternoon Break | | | |
| | 3:15pm-5:15pm | **Session 3A**<br>Functional Verification and Test Generation<br>Room: San Carlos | **Session 3B**<br>Power Delivery and Distribution<br>Room: San Juan | **Session 3C**<br>Quality System Level Design and Synthesis<br>Room: San Martin | |
| | 5:15pm-6:50pm | **Session 4A**<br>DFM for Circuit Design<br>Room: San Carlos | **Session 4B**<br>Leakage and Reliability Management<br>Room: San Juan | **Session 4C**<br>Analog Test and BIST<br>Room: San Martin | |
| | 7:00pm-9:00pm | **Evening Panel Discussion EP2**<br>**Nanoelectronics: Evolution or Revolution?** | | | |
| **Wednesday 3/23/05** | 8:30am-10:15am | **PLENARY SESSION 2P**<br>**Keynote Speeches by:**<br>**Jim Miller, Kurt A. Wolf, Bernard Candaele** | | | |
| | 10:15am-10:30am | Morning Break | | | |
| | 10:30am-12:00pm | **SESSION 5A**<br>Design Methods and Tools in DSM<br>Room: San Carlos | **SESSION 5B**<br>Design Techniques for Leakage Reduction<br>Room: San Juan | **SESSION 5C**<br>Variability Issues in Nanoscale Circuits<br>Room: San Martin | |
| | 12:00pm-1:00pm | **LUNCH BREAK** | | | |
| | 1:00pm-3:05pm | **SESSION 6A**<br>Issues in Noise and Timing<br>Room: San Carlos | **SESSION 6B**<br>Design Approaches for System in Package (SiP)<br>Room: San Juan | **SESSION 6C**<br>DSM Interconnect Issues<br>Room: San Martin | |
| | 3:05pm-3:30pm | Afternoon Break | | | |
| | 3:30pm-5:35pm | **SESSION 7A**<br>Advances in Floor Planning<br>Room: San Carlos | **SESSION 7B**<br>Issues in On-Chip Communication and Analog/RF Designs<br>Room: San Juan | **SESSION 7C**<br>Robust Design under Parameter Variations<br>Room: San Martin | |

# TUTORIALS
## San Carlos/San Juan

### TUTORIAL I
*9:00am-12:00pm*

## Design of sub-90nm Circuits and Design Methodologies

*Chair & Moderator*:
***Anirudh Devgan, IBM Research***

*Speakers:*
***Ruchir Puri**, Research Staff Member, IBM TJ Watson Research Center, NY*
***Sachin Sapatnaker,** Professor, Electrical & Computer Engineering, University of Minnesota*
***Tanay Karnik,** Principal Engineer, Intel Circuit Research Labs, Hillsboro, OR*
***Rajiv Joshi,** Research Staff Member, IBM T J Watson Research Center, NY*

***SUMMARY:***
This tutorial discusses design challenges of scaled CMOS circuits in sub-90nm technologies and the design methodologies required to design them in order to produce robust designs with desired power performance trade-off. We will focus on four major components:
Design challenges of sub-90nm CMOS circuits with particular emphasis on implications of each individual device scaling element on circuit design: To continue scaling of the CMOS devices deep into sub-90nm technologies, fully depleted SOI, strained-Si on SiGe, FinFETs with double gate, and even further, three-dimensional circuits will be utilized to design high-performance circuits. We will discuss unique design aspects and issues resulting from this scaling such as gate-to-body tunneling, self-heating, reliability issues, and process variations. As the scaling approaches various physical limits, new design issues such as Vt modulation due to leakage, low-voltage impact ionization, and higher $Vt_{lin}$ to maintain adequate $Vt_{sat}$, continue to surface. In this part of tutorial, we will discuss these emerging trends and design issues related to aggressive device scaling.

*Design methodologies for implementing robust circuits with desired power performance characteristics:* With device dimensions approaching their physical limits, design methodologies are playing increasing significant role in achieving desired power and performance. In deep-submicron designs, chip performance is increasingly limited by the interconnect delay. Transistor delays decrease with technology scaling, while the narrower metal lines and space increase the relative delay associated with the interconnects. As the designs are scaled to the next technology generation, the capacity of a same-sized die doubles, and the complexity and gate count of the design grows. This results in devices and interconnects wires being placed in ever-increasing proximity. As a result, the cross-coupling capacitance between adjacent wires is increasing with each technology generation. All of these trends indicate that interconnect delays in sub-90nm technologies will continue to dominate the overall chip performance. The dominant interconnect delays require accurate net length and delay prediction during timing optimization to improve circuit performance. Not only does the design of circuits in sub-90nm technologies require a high-performance logic synthesis system but it also necessitates seamless integration of placement and synthesis design environments. In addition, with the coupling-capacitance issues generating increasing difficulties for design closure, more accurate wire routes must be known while optimizing the design in order to fix these problems earlier in the design cycle. This requires close integration of interconnect routing environment with placement and synthesis environments. In this part of tutorial, we will present the details of a high-performance synthesis system and a design flow in which placement, synthesis, and routing environments closely and seamlessly interact with each other to handle flat designs that are over 5 million gates with fast turn around design times in 90nm CMOS technology.

*Managing leakage power:* It is well known that with CMOS technologies beyond 90nm, leakage power is one of the most crucial design components which must be efficiently controlled in order to utilize the performance advantage from these technologies. We will focus on various techniques to analyze and control all components of leakage power placing particular emphasis on sub-threshold and gate leakage power. In addition, this part of tutorial will discuss low voltage circuit design under high intrinsic leakage, leakage monitoring and control techniques, effective transistor stacking, multi-threshold CMOS, dynamic threshold CMOS, well biasing techniques, and design of low leakage data-paths and caches.

*Circuit Design in the Presence of Uncertainty:* Nanometer design technologies must work under tight operating margins, and are therefore highly susceptible to any process and environmental variabilities. This part of the tutorial will consider several factors related to reliability and yield. With regard to environmental variations, it is important to build circuits that have well-distributed thermal properties, and to carefully design supply networks to provide reliable Vdd and ground levels throughout the chip. On the process variation front, the effects of uncertainties in process variables must be modeled using statistical techniques, and they must be utilized to determine variations in the performance parameters of a circuit. Instead of pessimistically treating timing in a worst-case manner as is conventionally done in static timing analysis, statistical techniques will have to be employed that directly predict the percentage of circuits that are likely to meet a timing specification.

**TUTORIAL II**
*1:00pm-5:00pm*

## Modeling and Design of Chip-Package Interface

*Chair & Moderator*:
***Anirudh Devgan, IBM Research***

***Speakers:***
***Luca Daniel,*** *Massachusetts Institute of Technology, Cambridge, MA*
***Byron Krauter,*** *IBM Microelectronics, Austin, TX*
***Lei He,*** *UCLA EE Dept, Los Angeles, CA*

***SUMMARY:***
Signal integrity (SI) and power integrity are forecasted to be paramount issues for future chip and package designs. Larger number of IOs, higher frequencies, and tighter noise margins necessitate the merging of the design paradigms for chip IO and package. In this tutorial, we will shed light on a new chip-package co-design paradigm and all the technologies necessary to enable it. We will first discuss parameterized reduced order models accounting for all high frequency SI effects in the package that can be reliably and automatically extracted by field solvers. We will then introduce package-aware chip IO planning and placement, which is the key to chip-packaging co-design. Finally, we will cover detailed power and signal integrity modeling and optimization in package.

# Session EP1
# Panel Discussion & Dinner

**Donner Pass Room**
*6:30pm - 8:30pm*

## IP Creation and Use
## What roadblocks are ahead or it is just clear and bumpy road?

*Panel Organizer:* ***Pallab Chatterjee****, SiliconMap*
*Panel Moderator:* ***Stephen Ohr,*** *EETimes*

As custom (Analog & MS device level) design progresses into smaller process geometries, companies are faced with many challenges with new names - DFM, DFY, DIR, OPC/RET/MDP, DR and new tools in the EDA/CAD space. A great many of the issues have been around since the start of the IC industry; they are just getting new attention. This panel of seasoned veterans and technology innovators will discuss the change in the scope of the work effort involved in custom design in the 180-47nm process technologies and if the design superhighway has turned into a dead end with insurmountable roadblocks or simply a very bumpy side road in need of significant repair and upgrade.

***Panelists:***
***Joachim Kunkel,*** *Vice President of Engineering, DesignWare, Synopsys*
***Naveed Sherwani,*** *Co-Founder, President & CEO of Open-Silicon*
***Kevin MacLean****, Vice President, PDF Solutions*
***Jeff Lewis****, Ciranova*
***Mark Rubin,*** *Intersil Corp*
***Ken Brock****, Silvaco Data Systems*

# Plenary Session 1P

## Donner Pass Room

***8:30AM - 10:15AM***

*Co-Chairs:* ***Kris Verma***
*Silicon Valley Technical Institute*
***Kenneth Shepard***
*Columbia University*

*8:30am*
**Introduction & Announcements**

*8:45am*
## 1P.1 Enabling True Design for Manufacturability

**John Kibarian**
President & CEO, PDF Solutions

Without any doubt, Design For Manufacturability has been the hottest buzzword for the last couple of years. This is quite justifiable by the enormous challenges in nanometer technology nodes and ever increasing design-process interactions. As a result, virtually all EDA companies have focused on providing the "DFM Solutions". Since the concept of DFM covers an extremely broad spectrum of tasks from the system level all the way to the manufacturing process, many of these DFM solutions are just the re-labeled design verification tasks.
In this talk, we will provide a more thorough classification of various DFM activities with the emphasis on the design tasks. We will also discuss the necessary condition to enable true DFM, i.e., the comprehensive characterization of the design-process interactions. We will present a complete process characterization methodology that is capable of extracting all the salient process variations for a full set of product design attributes. We will illustrate our talk by showing the yield loss Pareto for the leading technology nodes that will cover all the dominant yield loss phenomena including random, systematic and parametric mechanisms. We will also demonstrate example of design flows that take advantage of such a comprehensive characterization together with silicon results demonstrating the advantages of true DFM.

*9:15am*
## 1P.2 Recent progress and remaining challenges in pattern transfer technologies for advanced chip designs

**Ashok K. Sinha**
Sr. VP & GM
Applied Materials, Inc

Even as the Moore's law continues to drive "tiny technologies" through relentless scaling, the main technology driver for semiconductor chips has evolved from DRAMs to Microprocessors to FPGAs. The underlying metrics have evolved from bits per chip and cost per bit for computers to functions per chip and cost per function for consumer products. This talk will review the remarkable progress that has been made in enabling pattern transfer technologies, including mask design, lithography enhancements and precision etching on the new 300mm wafers for an increasingly wide variety of new materials. However, there is a cost associated with all this and the cost-benefit tradeoffs will almost certainly drive new inflections in the entire food chain, which I will try to identify.

*9:45am*
## 1P.3 Shifting Perspectives on DFM

**Joe Sawicki**
Vice President & General Manager
Mentor Graphics

In micron technologies, manufacturing constraints were captured in process technology rule files. This process information was accessed at different levels of abstraction during various stages in the design flow. In addition, design teams implemented best practice methodologies and ‘experience-based’ guidelines throughout the design chain to ensure acceptable yield and adequate test coverage.
So what changed in the quest for an optimum DFM methodology? Nanometer technology has ushered in new and significant yield and manufacturing considerations and constraints. The lack of major increase in yield improvement between the 350nm and 180nm nodes suggests that the yield loss mechanisms are not only increasing in numbers, magnitude, and complexity at each successive generation, but they are increasing at a rate fast enough to largely offset ‘cosmetic’ improvements in tools and methodologies.
If EDA tools are to assist the semiconductor industry at the 90nm and 65nm nodes, there must be profound changes to existing tools, and the introduction of new technologies that allow designers to consider and optimize for manufacturing at each stage of the design, verification, tapeout and test process.

Where will these new tools and capabilities appear? They will show up in all parts of the design flow, as well as on the manufacturing floor. In particular, an immediate focus for the EDA industry must center on delivering new technology in four key areas: process modeling (electrical and lithographic), statistical analysis and visualization, design optimization and Test and inspection.

# Session 1A

## San Carlos Room

***10:30AM - 12:05PM***

## Tools and Flows for Quality Design

*Chairs:* ***Tom Chen,*** *Colorado State University*
***Syed M. Alam****, Freescale Semiconductor*

*10:30am*
**Introduction**

*10:35am*
**1A.1**
**Toward High Quality Tools and Tool Flows Through High-Performance Computing**
*Aaron N.L. Ng, Igor L. Markov, University of Michigan*

*11:05am*
**1A.2**
**Noise Library Characterization for Large Capacity Static Noise Analysis Tools**
*Alex Gyure, Alireza Kasnavi, Sam Lo, Peivand F. Tehrani, William Shu, Mahmoud Shahram, Joddy W. Wang, Jindrich Zedja, Synopsys Inc.*

*11:35am*
**1A.3**
**Two-Dimensional Layout Migration by Soft Constraint Satisfaction**
*Qianying Tang, Jianwen Zhu, University of Toronto*

*11:50am*
**1A.4**
**Domain Strategy and Coverage Metric for Validation**
*Luo Chun, Yang Jun, Shi Longxing, Wu XuFan, Zhang Yu, Southeast University, China*

# Session 1B

## San Juan Room

***10:30AM - 12:05PM***

## High Level Power/Noise Reduction Techniques

*Chairs:* ***Farzan Fallah,*** *Fujitsu Laboratories of America*
***Norman Chang,*** *Apache Design Solutions*

*10:30 am*
**Introduction**

*10:35am*
**1B.1**
**Power Supply Noise-Aware Scheduling and Allocation for DSP Synthesis**
*Dongku Kang, Yiran Chen, Kaushik Roy, Purdue University*

*11:05am*
**1B.2**
**Reducing Power Consumption during TLB Lookups in a PowerPC Embedded Processor**
*Shivakumar Swaminathan, Sanjay B. Patel, James Dieffenderfer, Joel Silberman, IBM*

*11:35am*

**1B.3**
**TFT-LCD Application Specific Low-Power SRAM Using Charge-Recycling Technique**
*Kee-Jong Kim, Chris H. Kim, Kaushik Roy, Purdue University*

*11:50am*
**1B.4**
**Error Analysis for the Support of Robust Voltage Scaling**
*David Roberts*, Todd Austin*, David Blaauw*, Krisztian Flautner**, Trevor Mudge*, *University of Michigan, **ARM Ltd., UK*

# Session 1C

## San Martin Room

***10:30AM - 12:05PM***

## Leakage and Dynamic Power Issues

*Chairs:* ***Paul Tong,*** *Pericom Semiconductor*
***Naehyuck Chang,*** *Seoul National University*

*10:30am*
**Introduction**

*10:35am*
**1C.1**
**Analytical Study of Impact Ionization and Subthreshold Current in Submicron N-MOSFET**
*Bhavana Jharia, S. Sarkar R. P. Agarwal, Dept. of E& CE, Indian Institute of Technology, Roorkee-INDIA*

*11:05am*
**1C.2**
**Analysis and Optimization of Static Power Considering Transition Dependency of Leakage Current in VLSI Circuits**
*Afshin Abdollahi*, Farzan Fallah**, Massoud Pedram*, *University of Southern California, **Fujitsu Laboratories of America, Inc.*

*11:35am*
**1C.3**
**Controlled-Load Limited Switch Dynamic Logic Circuit**
*Jayakumaran Sivagnaname, Hung C. Ngo, Kevin J. Nowka, Robert K. Montoye, Richard B. Brown, University of Michigan*

*11:50am*
**1C.4**
**Dynamically Pulsed MTCMOS with Bus Encoding for Total Power and Crosstalk Minimization**
*Harmander S. Deogun, Rahul M. Rao, Dennis Sylvester, Richard Brown, Kevin Nowka, University of Michigan*

# Session 1D

## City Foyer

***10:30AM – 3:15PM***

## Poster Session

*Chairs:* ***James Lei****, Altera*
***Israel Koren,*** *University of Massachusetts Amherst*

**1D.1**
**Non-Charge-Sheet Core and Architecture of BSIM5**
*Jin He, Jane Xi, Mansun Chan, Hui Wan, Mohan Dunga, Babak Heydari,, Ali M. Niknejad, Chenming Hu, University of California, Berkeley*

**1D.2**
**Integration of DFM Practices in Design Flows**
*L.Riviere Cazaux, Freescale Semiconductors*

**1D.3**
**How Circuit Analysis and Yield Optimization Can Be Used to Detect Circuit Limitations before Silicon Results**
*Carlo Roma, Pierluigi Daglio, Guido De Sandre, Marco Pasotti, Marco Poles, STMicroelectronics*

**1D.4**
**Leakage Current Modeling in Pd SOI Circuits**
*Mini Nanua*, David Blaauw**, MI, Chanhee Oh***, *Sun Microsystems, Austin, TX, **University of Michigan, ***Nascentric, Austin, TX*

**1D.5**
**A Balanced Scorecard for Systemic Quality in Electronic Design Automation: An Implementation Method for an EDA Company**
*Jasjeet Kaur, Mentor Graphics*

**1D.6**
**RCL Characterization and Modeling of X Architecture Diagonal Wires for VLSI Design**
*Narain D. Arora, Li Song, Santosh Shah, Kalyan Thumaty, Aki Fujimura, Victor Chang*, S. Y. Cho*, Cadence Design Systems, *TSMC*

**1D.7**
**A Technique for Designing Totally Self-Checking Domino Logic Circuits**
*C.K. Tang, P.K. Lala, J.P. Parkerson, University of Arkansas*

**1D.8**
**Early Assessment of Leakage Power For System Level Design**
*C. Talarico, B.S. Pillilli, K.L.Vakata. J.M. Wang, University of Arizona*

**1D.9**
**Technology Mapping For Reliability Enhancement in Logic Synthesis**
*Zhaojun Wo, Israel Koren, University of Massachusetts Amherst*

**1D.10**
**Evaluation of Capacitor Ratios in Automated Accurate Common-Centroid Capacitor Arrays**
*Diaaeldin Khalil*, Mohamed Dessouky*, Vincent Bourguet**, Marie-Minerve Louërat**, Andreia Cathelin***, *Hani Ragai*
*Ain Shams University, Egypt, **University of Paris 6, France, ***STMicroelectronics, France*

**1D.11**
**Closing the Gap Between Carry Select Adder and Ripple Carry Adder: A New Class of Low-Power High-Performance Adders**
*Behnam Amelifard*, Farzan Fallah**, Massoud Pedram*, *University of Southern California, **Fujitsu Laboratories of America, Inc.*

**1D.12**
**Capacitance and Yield Evaluations Using a 90-Nm Process Technology Based on the Dense Power-Ground Interconnect Architecture**
*Atsushi Kurokawa, Masaharu Yamamoto, Nobuto Ono, Tetsuro Kage, Yasuaki Inoue, Hiroo Masuda, Semiconductor Technology Academic Research Center, Japan*

**1D.13**
**Testing for Resistive Shorts in FPGA Interconnects**
*Haixia Gao, Yintang Yang, Xiaohua Ma, Gang Dong, Xidian University, P.R. China*

**1D.14**
**TED Thermo-Electrical Designer: A New Physical Design Verification Tool**
*Sokolowska Ewa, Barszcz Marek, Kaminska Bozena, Pultronics Inc.*

**1D.15**
**A Fast Lithography Verification Framework for Litho-Friendly Layout Design**
*Yong-Chan Ban, Soo-Han Choi, Ki-Hung Lee, Dong-Hyun Kim, Ji-Suk Hong, Yoo-Hyon Kim, Moon-Hyun Yoo, Jeong-Taek Kong, Samsung, South Korea*

**1D.16**
**Gate-Level Mitigation Techniques for Neutron-Induced Soft Error Rate**
*Harmander S. Deogun, Dennis Sylvester, David Blaauw, University of Michigan*

**1D.17**
**Exact Algorithms for Coupling Capacitance Minimization by Adding One Metal Layer**
*Hua Xiang, Kai-Yuan Chao, Martin D.F. Wong, IBM*

**1D.18**
**Design of a 10-bit TSMC 0.25um CMOS Digital to Analog Converter**
*J. Huynh, B. Ngo, M. Pham, Lili He, San Jose State University*

**1D.19**
**A High-Performance SRAM Technology with Reduced Chip-Level Routing Congestion for SOC**
*R. Castagnetti, R. Venkatraman, B. Bartz, C. Monzel, T. Briscoe, A. Teene, S. Ramesh, LSI Logic*

**1D.20**
**Design and Evaluation of a Security Scheme for Sensor Networks**
*Khadija Stewart, Themistoklis Haniotakis, Spyros Tragoudas, Southern Illinois University Carbondale*

**1D.21**
**A Minimum Cut Based Re-Synthesis Approach**
*M. Welling, S.Tragoudas, H. Wang, Southern Illinois University Carbondale*

**1D.22**
**Analysis for Complex Power Distribution Networks Considering Densely Populated Vias**
*Young-Seok Hong, Heeseok Lee, Joon-Ho Choi, Moon-Hyun Yoo, Jeong-Taek Kong, Samsung Korea*

**1D.23**
**Buffer Planning Algorithm Based on Partial Clustered Floorplanning**
*Yuchun Ma, Xianlong Hong, Sheqin Dong, Song Chen, Chung-Kuan Cheng, Tsinghua University, China*

**1D.24**
**Issues and Challenges in Ramp to Production**
*Ravi Arora, Arun Shrimali, Anand Venkitachalam, Texas Instruments*

## ISQED Luncheon Awards & Speech

**Donner Pass Room**
*12:00pm-1:00pm*

*Chairs:* ***Ali Iranmanesh,*** *Silicon Valley Technical Institute*
***Kaustav Banerjee,*** *University of California at Santa Barbara*

*12:05pm*
**Committee Recognition Awards**
**Best Paper Awards** (Sponsored By Synopsys)

*12:25pm*
**Luncheon Speech:**

## IP Quality: A Design, not a Verification Problem

**Michael Keating**
Synopsys Inc.

## Session 2A

**San Carlos Room**
***1:00PM - 3:05PM***

### Test Application and Cost Reduction

*Chairs:* ***Sreejit Chakravarty,*** *Intel*
***David Bonyuet,*** *Delta Search Labs*

*1:00pm*
**Introduction**

*1:05pm*
**2A.1 Reseeding-Based Test Set Embedding With Reduced Test Sequences**
*E. Kalligeros, D. Kaseridis, X. Kavousianos, D. Nikolos, University of Patras, Greece*

*1:35pm*
**2A.2 Reduced Test Application Time Based On Reachability Analysis**
*Th. Haniotakis, S. Tragoudas, G. Pani, ECE Dept., Southern Illinois University*

*2:05pm*
**2A.3 Using MUXs Network to Hide Bunches of Scan Chains**
*Yinhe Han*, Yu Hu* *, Huawei Li* *, Xiaowei Li*, *Institute of Computing Technology, Chinese Academy of Sciences, Beijing, **Graduate School of Chinese Academy of Sciences, Beijing*

*2:35pm*
**2A.4 BIST-Guided ATPG**
*Ahmad A. Al-Yamani, Edward J. McCluskey, Stanford University*

*3:05pm*
**2A.5 Dynamic Test Compaction for Bridging Faults**
*Irith Pomeranz and Sudhakar M. Reddy, Purdue University*

# Session 2B

## San Juan Room

***1:00PM - 3:05PM***

## DFM and Physical Layout

*Chairs:* ***Enrico Malavasi,*** *PDF Solutions*
***Kris Verma****, Silicon Valley Technical Institute*

*1:00pm*
**Introduction**

*1:05pm*
**2B.1**
**A Min-Variance Iterative Method for Fast Smart Dummy Feature Density Assignment in Chemical-Mechanical Polishing**
*Xin Wang, Charles Chiang, Jamil Kawa, Qing Su, Synopsys Inc.*

*1:35pm*
**2B.2**
**Standard Cell Printability Grading and Hot Spot Detection**
*Michel Cote Philippe Hurat, Synopsys Inc.*

*2.05pm*
**2B.3**
**Performance Driven OPC for Mask Cost Reduction**
*Puneet Gupta*, Andrew B. Kahng*, Dennis Sylvester**, Jie Yang**, *University of California at San Diego, **University of Michigan*

*2.35pm*
**2B.4**
**Meeting Nanometer DPM Requirements through DFT**
*Jay Jahangiri, David Abercrombie, Mentor Graphics*

# Session 2C

## San Martin Room

***1:00PM - 3:05PM***

## Performance and Reliability Analysis for Yield Optimization

*Chairs:* ***Amir Ajami,*** *Magma Design Automation*
***Adrian Ionescu,*** *Swiss Federal Institute of Technology (EPFL)*

*1:00pm*
**Introduction**

*1:05pm*
**2C.1**
**Parametric Yield Analysis and Constrained-Based Supply Voltage Optimization**
*Rahul Rao, Kanak Agarwal, Anirudh Devgan, Dennis Sylvester, Richard Brown, Kevin Nowka, University of Michigan*

*1:35pm*
**2C.2**
**Power-Delay Metrics Revisited for 90nm CMOS Technology**
*Dipanjan Sengupta, Resve Saleh, University of British Columbia, Canada*

*2.05pm*
**2C.3**
**Optimization of Individual Well Adaptive Body Biasing (IWABB) Using a Multiple Objective Evolutionary Algorithm**
*Justin Gregg, and Tom W. Chen, Colorado State University*

*2.35pm*
**2C.4**
**Electromigration Reliability Comparison of Cu and Al Interconnects**
*Syed M. Alam*, Frank L. Wei, Chee L. Gan**, Carl V. Thompson, Donald E. Troxel, *Freescale Semiconductor, **Nanyang Technological University, Massachusetts Institute of Technology*

# Session 3A

## San Carlos Room

***3:15PM - 5:15PM***

## Functional Verification and Test Generation

*Chairs:* ***Daniela De Venuto,*** *Politecnico di Bari, Italy*
***George Alexiou,*** *University of Patras and Computer Technology Institute, Greece*

*3:15pm*
**Introduction**

*3:20pm*
**3A.1**
**Combining System Level Modeling with Assertion Based Verification**
*Anat Dahan*, Daniel Geis*t, Leonid Gluhovsky*, Dmitry Pidan*, Gil Shapir*, Yaron Wolfsthal*, Lyes Benalycherif**, Romain Kamdem**, Younes Lahbib**, *IBM Haifa Research Lab, Haifa Israel, **STMicroelectronics, Grenoble, France*

*3:50pm*
**3A.2**
**Low Voltage Test In Place of Fast Clock in DDSI Delay Test**
*Haihua Yan, Gefu Xu, Adit D. Singh, Auburn University*

*4:20pm*
**3A.3**
**Functional Verification of Networked Embedded Systems**
*Nicola Bombieri, Franco Fummi, Graziano Pravadelli*

*4:50pm*
**3A.4**
**Functions for Quality Transition Fault Tests**
*Maria K. Michael*, Stelios Neophytou*, Spyros Tragoudas**, *University of Cyprus, **Southern Illinois University, Carbondale*

# Session 3B

## San Juan Room

***3:15PM - 5:15PM***

## Power Delivery and Distribution

*Chairs:* ***Ravi Joshi,*** *IBM*
***David Overhauser,*** *Cadence Design Systems*

*3:15pm*
**Introduction**

*3:20pm*
**3B.1**
Noise Aware Decoupling Capacitors for Multi-Voltage Power Distribution Systems
*Mikhail Popovich, Eby G. Friedman, University of Rochester*

*3:50pm*
**3B.2**
P/G Pad Placement Optimization: Problem Formulation for Best IR Drop
*Aishwarya Dubey, Texas Instruments*

*4:20pm*
**3B.3**
Impact of On-Chip Inductance on Power Distribution Network Design for Nanometer Scale Integrated Circuits
*Navin Srivastava, Xiaoning Qi, Kaustav Banerjee, University of California at Santa Barbara*

*4:50pm*
**3B.4**
Power Grid Planning for Microprocessors and SOCs
*Qing K. Zhu*

# Session 3C

## San Martin Room

***3:15PM - 5:15PM***

## Quality System Level Design and Synthesis

*Chairs:* ***Lech Jozwiak,*** *Eindhoven University of Technology, The Netherlands*
***Artur Chojnacki,*** *PDF Solutions*

*3:15pm*
**Introduction**

*3:20pm*
**3C.1**
**A Power-Aware GALS Architecture for Real-Time Algorithm-Specific Tasks**
*Animesh Datta, Swarup Bhunia, Nilanjan Banerjee, Kaushik Roy, Purdue University*

*3:50pm*
**3C.2**
**An ILP Formulation for Reliability-Oriented High-Level Synthesis**
*Suleyman Tosun*, Ozcan Ozturk**, Nazanin Mansouri*, Ercument Arvas*, Mahmut Kandemir**, Yuan Xie**,*Syracuse University, **Pennsylvania State University*

*4:20pm*
**3C.3**
**Analysis of the Effect Of LUT Size on FPGA Area and Delay Using Theoretical Derivations**
*Haixia Gao, Yintang Yang, Xiaohua Ma, Gang Dong, Xidian University, China*

*4:50pm*
**3C.4**
**Reliability-Centric Hardware/Software Co-Design**
*Suleyman Tosun*, Nazanin Mansouri*, Ercument Arvas*, Mahmut Kandemir**, Yuan Xie**, *Syracuse University, **Pennsylvania State University*

# Session 4A

## San Carlos Room

***5:15PM – 6:50PM***

## DFM for Circuit Design

*Chairs:* ***Sani Nassif,*** *IBM*
***Nagib Hakim,*** *Intel*

*5:15pm*
**Introduction**

*5:20pm*
**4A.1**
**Deep Submicron CMOS Integrated Circuit Reliability Simulation with SPICE**
*Xiaojun Li, B. Huang, J. Qin, X. Zhang, M. Talmor, Z. Gur, Joseph B. Bernstein, University of Maryland*

*5:50pm*
**4A.2**
**Modeling Layout Effects for Sensitivity-based Analog Circuit Optimization**
*Henry H. Y. Chan, Zeljko Zilic, McGill University*

*6:20pm*
**4A.3**
**In-Circuit Self-Tuning of Clock Latencies**
*Kambiz Rahimi*, Chris Diorio**, *Impinj Inc., **University of Washington*

*6:35pm*
**4A.4**
**Statistical Analysis of Clock Skew Variation in H-tree Structure**
*Masanori Hashimoto, Tomonori Yamamoto, Hidetoshi Onodera, Osaka University, Japan*

# Session 4B

## San Juan Room

***5:15PM – 6:50PM***

## Leakage and Reliability Management

*Chairs:* ***Panda Rajendran,*** *Freescale Semiconductor*
***Seung H. Kang,*** *Agere Systems*

*5:15pm*
**Introduction**

*5:20pm*
**4B.1**
**Modeling and Analysis of Gate Leakage In Ultra-Thin Oxide Sub-50nm Double Gate Devices And Circuits**
*Saibal Mukhopadhyay*, Keunwoo Kim**, Jae-Joon Kim**, Shih-Hsien Lo**, Rajiv V. Joshi**, Ching-Te Chuang**, Kaushik Roy*, *Dept. Of ECE, Purdue University, **IBM T. J. Watson Research Center, Yorktown Heights*

*5:50pm*
**4B.2**
**Design for Degradation: Cad Tools for Managing Transistor Degradation Mechanisms**
*G Ananth Somayaji, Gautam Kapila, Texas Instruments*

*6:20pm*
**4B.3**
**A Practical Transistor-Level Dual Threshold Voltage Assignment Methodology**
*Puneet Gupta, Andrew B. Kahng, Puneet Sharma, University of California at San Diego*

*6:35pm*
**4B.4**
**Analysis and Design of LVTSCR-Based EOS/ESD Protection Circuits for Burn-In Environment**
*O. Semenov, H. Sarbishaei, M. Sachdev, University of Waterloo*

# Session 4C

## San Martin Room

***5:15PM – 6:50PM***

## Analog Test and BIST

*Chairs:* ***Spyros Tragoudas,*** *Southern Illinois University Carbondale*
***Li-C Wang,*** *University of California at Santa Barbara*

*5:15pm*
**Introduction**

*5:20pm*
**4C.1**
**Built-In-Self-Testing Techniques for Programmable Capacitor Arrays**
*Amit Laknaur, Haibo Wang, Southern Illinois University Carbondale*

*5:50pm*
**4C.2**
**A Co-design Tool to Validate And Improve an FPGA Based Test Strategy for High Resolution Audio ADC**
*Daniela De Venuto, Grazia Marchione, Leonardo Reyneri, Politecnico di Bari, Italy*

*6:20pm*
**4C.3**
**A Built-In Self-Test Scheme for Differential Ring Oscillators**
*Dermentzoglou Lampros, Tsiatouhas Yiorgos, Arapoyanni Angela, National and Kapodistrian University of Athens*

*6:35pm*
**4C.4**
**Power Reduction in Test-Per-Scan BIST with Supply Gating and Efficient Scan Partitioning**
*Swarup Bhunia, Hamid Mahmoodi, Kaushik Roy, Purdue University*

# Session EP2
# Panel Discussion & Dinner

## Donner Pass Room

*7:00PM -9:00PM*

## Nanoelectronics: Evolution or Revolution?

*Panel Organizer**: Ali Keshavarzi, Intel***
*Panel Moderator: **(tbd)***

Scaling of CMOS technology continues in spite of tremendous technology development barriers, design challenges and prohibitive costs. Today, the 65nm CMOS technology node is moving from development to high volume manufacturing while research and development continues on future technology nodes including 45nm, 30nm and beyond. Design of ICs in these scaled technologies faces new limitations. It is increasingly difficult to sustain supply and threshold voltage scaling to provide the required performance increase, limit energy consumption, control power dissipation, and maintain reliability. These requirements pose several difficulties across a range of disciplines spanning technology, fabrication, transistor structure, circuits, systems, design, and architecture.

On the technology front, the question arises whether we can continue to scale CMOS technology and whether we are close to the end of the ITRS roadmap. Are there any fundamental barriers? Should we continue along the traditional CMOS scaling path - reduce effective oxide thickness, improve channel mobility, and minimize parasitic - or consider a more radical departure from planar CMOS to non-planar device structures such as tri-gate and FinFET thin body transistors? Will we ever use nanowires and other novel nano devices such as Carbon nanotubes and self-assembled molecular devices? How important is self-assembly and bottom-up manufacturing in making future systems? What options do we have post non-planar CMOS and before more exotic spintronics and quantum devices? On the design front, while researchers are addressing various circuit design techniques to deal with process variation and leakage, it is unclear whether we can build systems with non-planar CMOS devices and other novel nano devices. Do we need new circuit design methods? How do we put systems together either with aggressively scaled Si devices, non-planar CMOS or with self-assembled molecular devices? What are the implications for design community? Will the information processing paradigm shift? Will we learn anything from researching futuristic nanoscale devices, circuits and systems that may impact scaling of Silicon CMOS technology?

***Panelists:***
***Mark Lundstrom**, Purdue University*
***Philip Wong**, Stanford University and formerly IBM*
***Kazuo Yano**, Hitachi - Research*

# Plenary Session 2P

## Donner Pass Room

***8:30AM - 10:15AM***

*Co-Chairs:* ***Kris Verma***
*Silicon Valley Technical Institute*
***Lech Jozwiak***
*Eindhoven University of Technology, The Netherlands*

*8:30am*
**Introduction & Announcements**

*8:45am*
**2P.1**
## Quality and EDA

**Aki Fujimura**
Chief Technology Officer
Cadence Design Systems

Quality has many definitions. Conformance to specifications; Customer Satisfaction; Delivery divided by Expectations; etc. EDA's sense of quality is determined by what it's customers want. Do we have a virtuous cycle in the quality relationship between EDA and its customers? EDA is also the quality tools supplier to help the Electronics Systems and semiconductor companies to produce quality products on time. The speaker will examine both aspects of the quality issue from an EDA perspective.

*9:15am*
**2P.2**
## IP Quality: A New Model that Faces Methodology and Management Challenges

**Kurt A. Wolf**
Director, Library Management Division
TSMC

The promised value and productivity from re-aggregating the IC design chain isn't always delivered, in part because of isolated IP product development/quality related practices, and in part because of an inability, from a design management perspective, to see "big picture" issues in the IP marketplace. However, these challenges are not insurmountable.
The concern over IP quality has rightfully grown over the past years as the future growth of the IC industry depends on two factors; a) achieving higher levels of design productivity and b) shifting internal resources towards creating and delivering value-added user benefits that stimulate increased end-product consumption. While the second factor is not discussed in this presentation, there's a presumption that higher IP quality and productivity enables a shift of resources to more applications-oriented design.
A pre-requisite to achieving the productivity gains is substantial improvements in the level of IP quality, coupled with increased forethought during product development. This presentation describes a methodology to evaluate IP for SOC integration. The focus is on development & quality verification practices that also account for the issues of IP integration.
Additionally, the long-term growth of the semiconductor industry may be limited by the lack of value placed on collaboration, support, quality verification, and due diligence between SOC design teams and their IP partners.
This presentation also describes improvements in the Hard IP business relationship between these groups that enable dramatic growth through slight changes in communications models.
By developing reasonable expectations and focusing on open discussion between each group, perspective begins to shift. The true value of the design team and IP partnership is a function of successful collaborations – not when the user squeezes the last drop out of NRE, royalty, per-use, or other financing models. And the value-add of the partnership is realized when that collaboration includes additional real, shared incentives that more fully value the IP industry, rather than focus on purely lowest cost.

*9:45am*
**2P.3**
## SoC Engineering Trends as Impacted by New Applications and System Level Requirements

**Bernard Candaele**
Department Head, SoC, IC & EDA

Thales, Paris Colombes, France

The SoC increasing integration scale as well as the system and customer requirements are important factors for a complete revisit of the development models for electronic products. New customer models ask for software driven electronics. Software engineering is moving to a component-based and MDA development approach to be applied to embedded applications. Hardware engineering is moving to SSDI System Level Development and Reuse methodologies. The 2 approaches have now to be further developed and combined for next generations SoC's to get high quality and adaptable designs at a reasonable development cost. New application-level quality standards have also to be part of the complete development flow.
It is demonstrated through several examples these new methodologies: system engineering methodology on software radios (UML, PIM Platform Independent Model and PSM Platform Specific Model) and its current extension to the hardware parts (SCA, OCP potential extensions), system engineering in line with the Common Criteria development and qualification process for new security products (PP Protection Profile and ST Security Target,…), development and validation methodology in line with DO254 standard for new safety products in avionics (formal verifications, …). Impacts on SoC architectures and design techniques will be discussed during the talk.

# Session 5A

## San Carlos Room

***10:30AM - 12:00PM***

## Design Methods and Tools in DSM

*Chairs:* ***Vamsi Srikantam****, Agilent Laboratories*
***James Lei,*** *Altera*

*10:30am*
**Introduction**

*10:35am*
**5A.1**
**ASLIC: A Low Power CMOS Analog Circuit Design Automation**
*Jihyun Lee, Yong-Bin Kim*

*11:05am*
**5A.2**
**Modeling MOS Snapback for Circuit-Level ESD Simulation Using BSIM3 and VBIC Models**
*Yuanzhong (Paul) Zhou, Duane Connerney, Ronald Carroll, Timwah Luk, Fairchild Semiconductor*

*11:35am*
**5A.3**
**A Mask Reuse Methodology for Reducing System-on-a-Chip Cost**
*Subhrajit Bhattacharya, John A Darringer, Daniel L. Ostapko, Youngsoo Shin, IBM*

# Session 5B

## San Juan Room

***10:30AM - 12:00PM***

## Design Techniques for Leakage Reduction

*Chairs:* ***David Overhauser,*** *Cadence Design Systems*
***Adrian Ionescu,*** *Swiss Federal Institute of Technology (EPFL)*

*10:30am*
**Introduction**

*10:35am*
**5B.1**
**Design of High Performance Sense Amplifier Using Independent Gate Control in sub-50nm Double-Gate MOSFET**
*Saibal Mukhopadhyay, Hamid Mahmoodi, Kaushik Roy, Purdue University*

*11:05am*
**5B.2**
**Simulating and Improving Microelectronic Device Reliability by Scaling Voltage and Temperature**
*Xiaojun Li, Joerg D. Walter, Joseph B. Bernstein, University of Maryland*

*11:35am*
**5B.3**
**Predicting and Designing for the Impact of Process Variations and Mismatch on the Trim Range and Yield of Bandgap References**
*Vishal Gupta, Gabriel A. Rincon-Mora, Georgia Institute of Technology*

# Session 5C

## San Martin Room

***10:30AM - 12:00PM***

## Variability Issues in Nanoscale Circuits

*Chairs:* ***Sharad Saxena,*** *PDF Solutions*
***Nikos Konofaos,*** *University of Patras, Greece*

*10:30am*
**Introduction**

*10:35am*
**5C.1**
**Modeling Intrinsic Fluctuations in Decananometer MOS Devices due to Gate Line Edge Roughness (LER)**
*Norman Gunther*, Emad Hamadeh**, Darrell Niemann*, Iliya Pesic***, Mahmud Rahman*, * Santa Clara University, ** Applied Micro Circuits Corp., *** Silvaco*

*11:05am*
**5C.2**
**Modeling Within-Die Spatial Correlation Effects for Process-Design Co-Optimization**
*Paul Friedberg, Yu Cao, Jason Cain, Ruth Wang, Jan Rabaey, Costas Spanos, University of California at Berkeley*

*11:35am*
**5C.3**
**Robust Multi-Level Current-Mode On-Chip Interconnect Signaling in the Presence of Process Variations**
*Vishak Venkatraman, Wayne Burleson, University of Massachusetts Amherst*

# Session 6A

## San Carlos Room

***1:00PM - 3:05PM***

## Issues in Noise and Timing

*Chairs:* ***Rajeev Murgai,*** *Fujitsu Laboratories of America*
***Eileen You,*** *Cadence Design Systems*

*1:00pm*
**Introduction**

*1:05pm*
**6A.1**
**A Comprehensive Methodology for Noise Characterization of ASIC Cell Libraries**
*Sreeram Chandrasekar, Gaurav Kumar Varshney, V. Visvanathan, Texas Instruments*

*1:35pm*
**6A.2**
**Sensitivity-Based Gate Delay Propagation in Static Timing Analysis**

*Shahin Nazarian*, Massoud Pedram*, Emre Tuncer**, Tao Lin**, *University of Southern California, **Magma Design Automation*

*2:05pm*
**6A.3**
**Fast Decap Allocation Algorithm for Robust On-Chip Power Delivery**
*Zhenyu Qi*, Hang Li*, Sheldon X.-D. Tan*, Lifeng Wu**, Xianlong Hong***, *University of California Riverside, **Cadence, Yici Cai***, ***Tsinghua Univiversity, China*

*2:35pm*
**6A.4**
**Clock trees: differential or single ended?**
*Deepak Sekar, Georgia Institute of Technology*

# Session 6B

## San Juan Room

***1:00PM - 3:05PM***

## Design Approaches for System in Package (SiP)

*Chairs:* ***Lalitha Immaneni,*** *Intel*
***Ravi Mahajan,*** *Intel*

*1:00pm*
**Introduction**

*1:05pm*
**6B.1**
**Exploring the challenges in creating a high-quality mainstream design solution for System-in-Package (SiP) design**
*Bill McCaffrey, Cadence Design Systems*

*1:35pm*
**6B.2**
**Design and Analysis of Area-IO DRAM/Logic integration with System-in-a-Package**
*Anru Wang, Wayne Dai, University of California at Santa Cruz*

*2:05pm*
**6B.3**
**Physical Design of Optoelectronic System-On-A-Package: A Cad Tool and Algorithms**
*Chung-Seok(Andy) Seo, Abhijit Chatterjee, Nan M. Jokerst*

*2:35pm*
**6B.4**
**Concurrent Chip Package Design for Global Clock Distribution Using Standing Wave Approach**
*Meigen Shen, Li-Rong Zheng, Hannu Tenhunen*

# Session 6C

## San Martin Room

***1:00PM - 3:05PM***

## DSM Interconnect Issues

*Chairs:* ***Farzan Fallah,*** *Fujitsu Laboratories of America*
***Norman Chang,*** *Apache Design Solutions*

*1:00pm*
**Introduction**

*1:05pm*
**6C.1**
**Current Calculation on Signal Interconnects**
*Muzhou Shao, Youxin Gao, Lipen Yuan, Martin Df Wong, Hungming Chen, Synopsys Inc.*

*1:35pm*
**6C.2**
**Dummy Filling Methods for Reducing Interconnect Capacitance and Number of Fills**
*Atsushi Kurokawa, Toshiki Kanamoto, Tetsuya Ibe, Akira Kasebe, Chang Wei Fong, Tetsuro Kage, Yasuaki Inoue, Hiroo Masuda, STARC Japan*

*2:05pm*
**6C.3**
**Voltage Scaling, Wire Sizing and Repeater Insertion Design Rules for Wave-Pipelined VLSI Global Interconnect Circuits**
*Vinita V. Deodhar, Jeffrey A. Davis, Georgia Institute of Technology*

*2:35pm*
**6C.4**
**Interconnect Delay and Slew Metrics Using the First Three Moments**
*Jiaxing Sun, Yun Zheng, Qing Ye, Tianchun Ye*

*2:50pm*
**6C.5**
**Passive Hierarchical Model Order Reduction and Realization of RLCM Circuits**
*Pu Liu, Zhenyu Qi, Sheldon X.-D. Tan, University of California Riverside*

# Session 7A

## San Carlos Room

***3:30PM – 5:35PM***

## Advances in Floor Planning

*Chairs:* ***Marco Casale-Rossi,*** *STMicroelectronics*
***Tanay Karnik,*** *Intel*

*3:30pm*
**Introduction**

*3:35pm*
**7A.1**
**Reticle Floorplanning and Wafer Dicing for Multiple Project Wafers**
*Meng-Chiou Wu, Rung-Bin Lin, Yuan Ze University, Taiwan*

*4:05pm*
**7A.2**
**Obstacle-Avoiding Rectilinear Minimum-Delay Steiner Tree Construction towards IP-Block-Based SOC Design**
*Jingyu Xu, Xianlong Hong, Tong Jing, Yang Yang, Tsinghua University, China*

*4:35pm*
**7A.3**
**Wire Planning with Bounded Over-the-Block Wires**
*Hua Xiang, I-Min Liu, Martin D.F. Wong, IBM*

*5:05pm*
**7A.4**
**Floorplanning with Consideration of White Space Resource Distribution for Repeater Planning**
*Song Chen, Xianlong Hong, Sheqin Dong, Yuchun Ma, Chung-Kuan Cheng, Tsinghua University, China*

*5:20pm*
**7A.5**
**Thermal-Aware Floorplanning Using Genetic Algorithms**
*W. Hung, Y. Xie, N. Vijaykrishnan, C. Addo-Quaye, T. Theocharides, M. J. Irwin, Penn State University*

# Session 7B

## San Juan Room

***3:30PM – 5:35PM***

# Issues in On-Chip Communication and Analog/RF Designs

*Chairs:* ***Amit Mehrotra,*** *Berkeley Design Automation*
***George Alexiou,*** *University of Patras and Computer Technology Institute, Greece*

*3:30pm*
**Introduction**

*3:35pm*
**7B.1**
**Joint Equalization and Coding for On-Chip Bus Communication**
*Srinivasa R. Sridhara*, Ganesh Balamurugan**, Naresh R. Shanbhag*, *University of Illinois at Urbana-Champaign, **Intel*

*4:05pm*
**7B.2**
**A More Effective $C_{eff}$**
*Sani R. Nassif*, Zhuo Li**, *IBM, **Texas A&M University*

*4:35pm*
**7B.3**
**An Interconnect Insensitive Linear Time-Varying Driver Model for Static Timing Analysis**
*Chung-Kuan Tsai, Malgorzata Marek-Sadowska, University of California at Santa Barbara*

*5:05pm*
**7B.4**
**Design a Band-pass Pseudo-2-path Switched Capacitor Ladder Filter**
*A. Zahabi, O. Shoaei, Y. Koolivand, University of Tehran, IRAN*

*5:20pm*
**7B.5**
**Design Considerations for Low-Power Ultra Wideband Radio Receivers**
*Payam Heydari, University of California, Irvine*

# Session 7C

## San Martin Room

***3:30PM – 5:35PM***

## Robust Design under Parameter Variations

*Chairs:* ***Ravi Joshi****, IBM*
***Sarma Vrudhula,*** *Arizona* ***State*** *University*

*3:30pm*
**Introduction**

*3:35pm*
**7C.1**
**A New Method for Robust Design of Digital Circuits**
*Dinesh Patil, Sunghee Yun, Seung-Jean Kim, Alvin Cheung, Mark Horowitz, Stephen Boyd, Stanford University*

*4:05pm*
**7C.2**
**Analysis and Synthesis of Staggered Twisted Bundle for Crosstalk Reduction**
*Hao Yu, Lei He, University of California at Los Angeles*

*4:35pm*
**7C.3**
**Analysis of Wave-Pipelined Domino Logic Circuit and Clocking Styles Subject to Parametric Variations**
*Wei Ling, Yvon Savaria, l'École Polytechnique de Montréal*

*5:05pm*
**7C.4**
**Impact of Interconnect Process Variations on Memory Performance and Design**
*Andres Teene, Bob Davis, Ruggero Castagnetti, Jeff Brown, Shiva Ramesh, LSI Logic*